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Allen et al.

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(54) **MULTIPLE-PATTERNED SEMICONDUCTOR DEVICE CHANNELS**

(71) Applicant: **International Business Machines Corporation**, Armonk, NY (US)

(72) Inventors: **David H. Allen**, Rochester, MN (US); **Douglas M Dewanz**, Rochester, MN (US); **David P. Paulsen**, Dodge Center, MN (US); **John E. Sheets, II**, Zumbrota, MN (US); **Kelly L. Williams**, Rochester, MN (US)

(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 189 days.

(21) Appl. No.: **13/836,335**

(22) Filed: **Mar. 15, 2013**

(65) **Prior Publication Data**

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Related U.S. Application Data

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(51) **Int. Cl.**
H01L 21/768 (2006.01)
H01L 23/528 (2006.01)
H01L 23/532 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 23/5283*** (2013.01); ***H01L 21/76816*** (2013.01); ***H01L 21/76831*** (2013.01); ***H01L 21/76877*** (2013.01); ***H01L 23/53295*** (2013.01); *H01L 2924/0002* (2013.01)

(58) **Field of Classification Search**
CPC H01L 21/76877; H01L 23/53295; H01L 23/528; H01L 23/5283; H01L 21/76829; H01L 21/76831; H01L 21/76816; H01L 23/522; H01L 21/76802; H01L 21/76834
USPC 438/668
See application file for complete search history.

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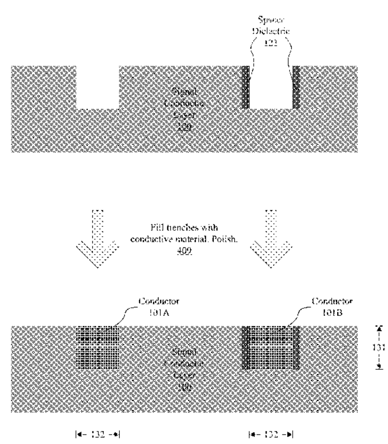
Primary Examiner — Khiem D Nguyen
Assistant Examiner — Pauline Vu
(74) *Attorney, Agent, or Firm* — Robert R. Williams; Nicholas D. Bowman

(57) **ABSTRACT**

A semiconductor device and method of manufacture are provided. The semiconductor device may include a multiple-patterned layer which may include multiple channels defined by multiple masks. A width of a first channel may be smaller than a width of a second channel. A conductor in the first channel may have a conductor width substantially equivalent to a conductor width of a conductor in the second channel. A spacer dielectric on a channel side may be included. The method of manufacture includes establishing a signal conductor layer including channels defined masks where a first channel may have a first width smaller than a second width of a second channel, introducing a spacer dielectric on a channel side, introducing a first conductor in the first channel having a first conductor width, and introducing a second conductor in the second channel having a second conductor width substantially equivalent to the first conductor width.

11 Claims, 29 Drawing Sheets



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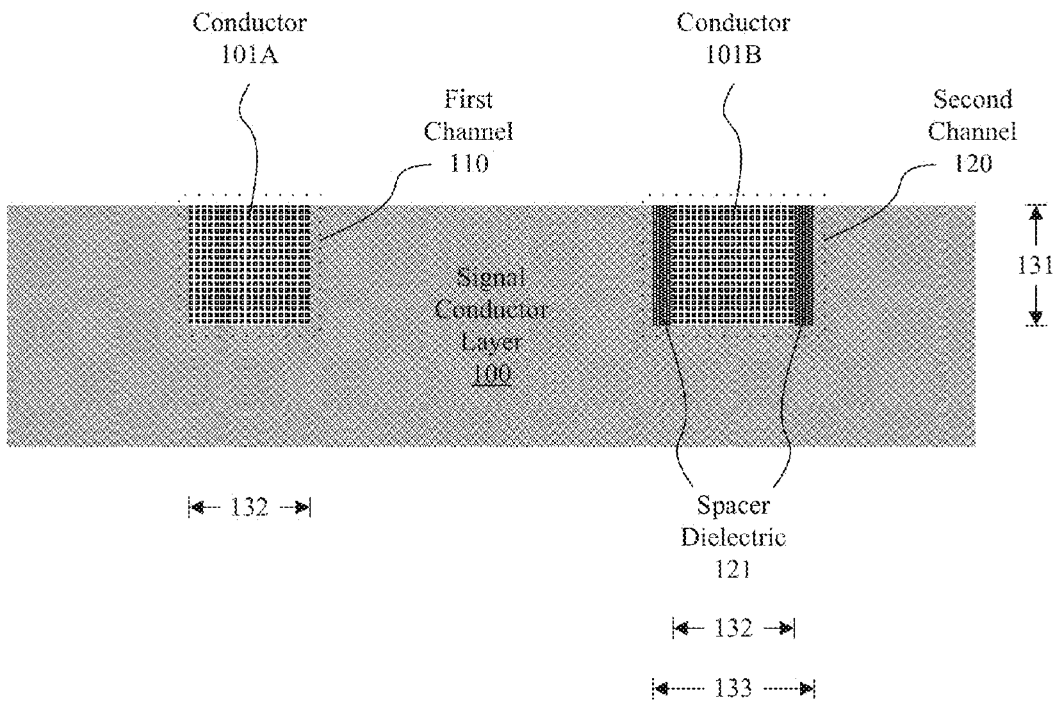

Conductor
101A
First
Channel
110
Conductor
101B
Second
Channel
120
131
Signal
Conductor
Layer
100
132
Spacer
Dielectric
121
132
133

FIG. 1

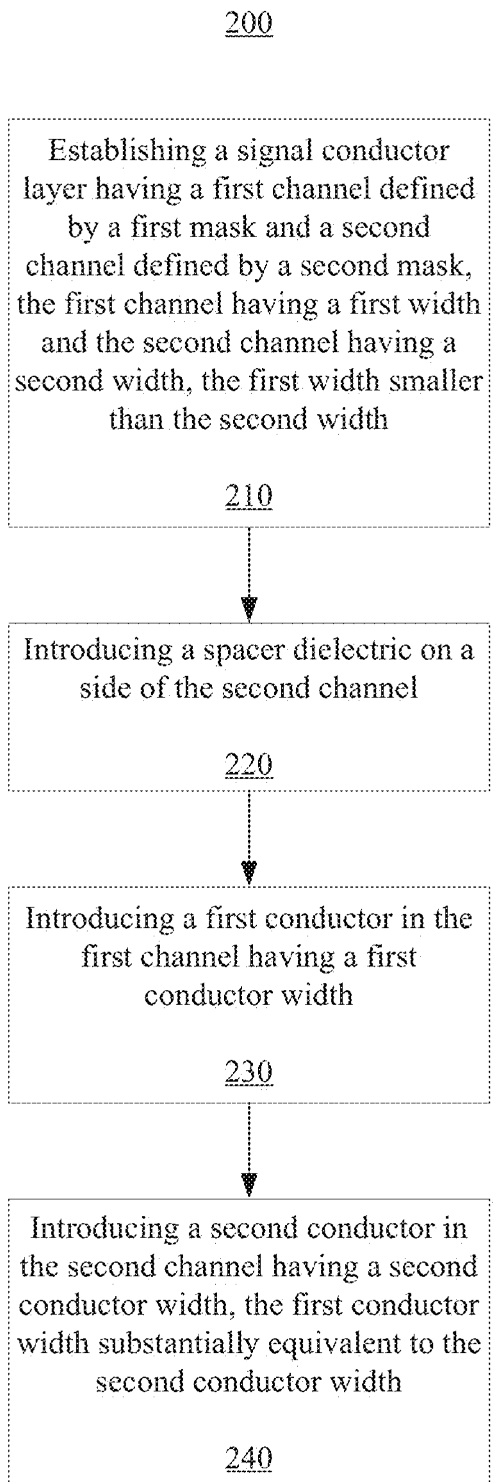

200
Establishing a signal conductor layer having a first channel defined by a first mask and a second channel defined by a second mask, the first channel having a first width and the second channel having a second width, the first width smaller than the second width
210
Introducing a spacer dielectric on a side of the second channel
220
Introducing a first conductor in the first channel having a first conductor width
230
Introducing a second conductor in the second channel having a second conductor width, the first conductor width substantially equivalent to the second conductor width
240

FIG. 2

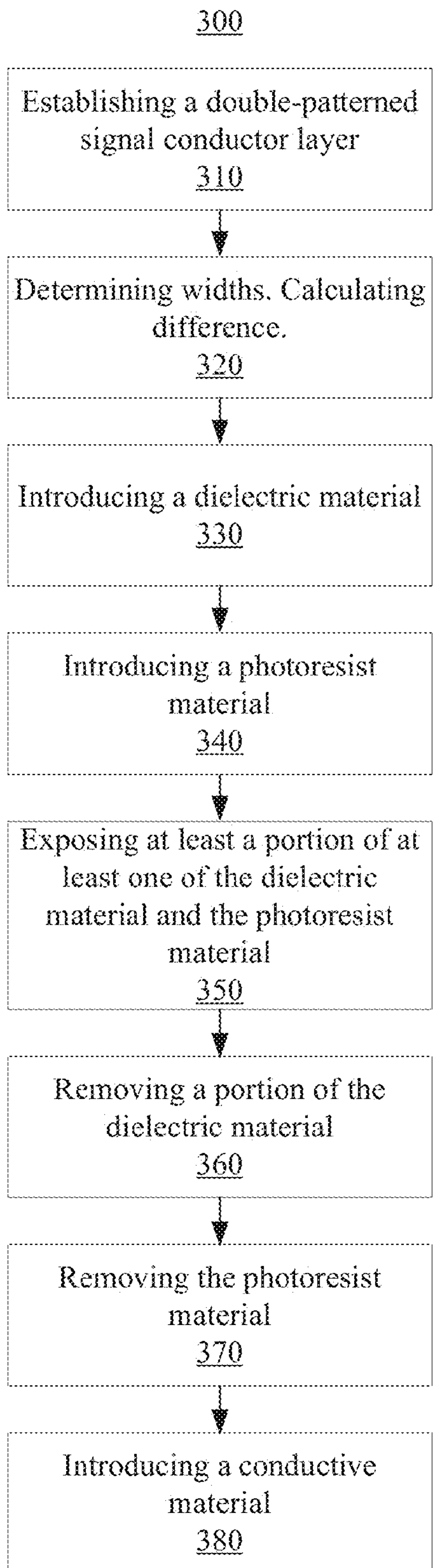

300
Establishing a double-patterned signal conductor layer
310
Determining widths. Calculating difference.
320
Introducing a dielectric material
330
Introducing a photoresist material
340
Exposing at least a portion of at least one of the dielectric material and the photoresist material
350
Removing a portion of the dielectric material
360
Removing the photoresist material
370
Introducing a conductive material
380

FIG. 3

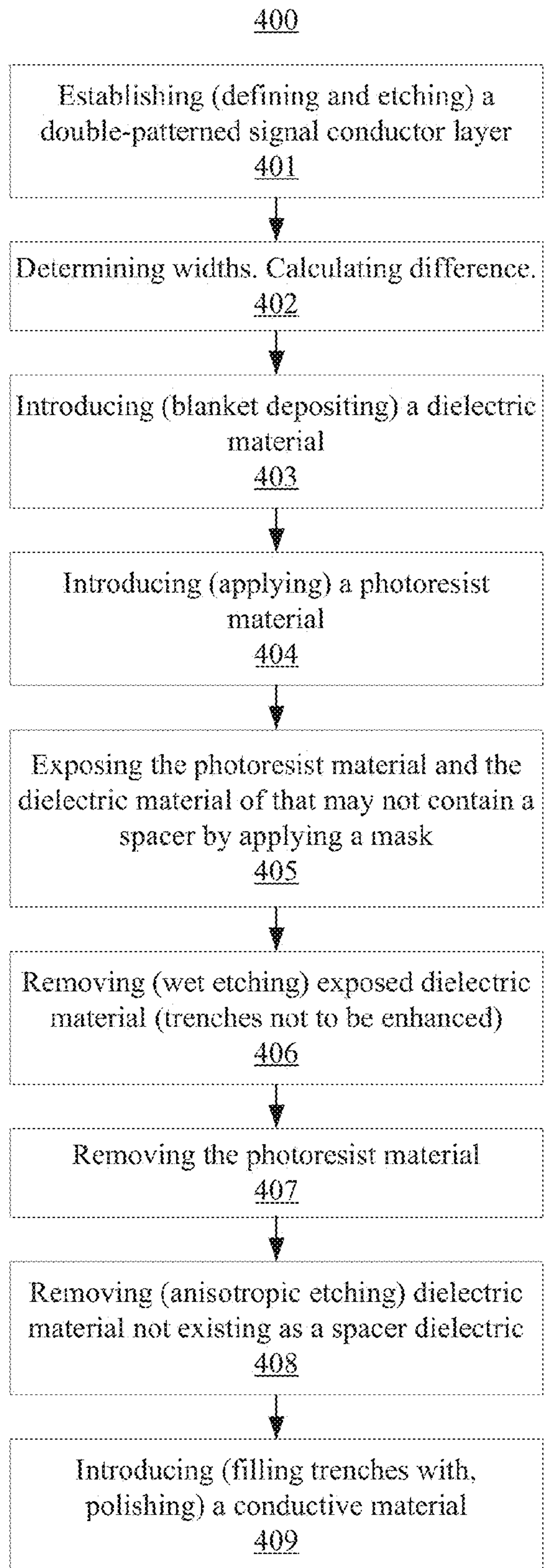

400
Establishing (defining and etching) a double-patterned signal conductor layer
401
Determining widths. Calculating difference.
402
Introducing (blanket depositing) a dielectric material
403
Introducing (applying) a photoresist material
404
Exposing the photoresist material and the dielectric material of that may not contain a spacer by applying a mask
405
Removing (wet etching) exposed dielectric material (trenches not to be enhanced)
406
Removing the photoresist material
407
Removing (anisotropic etching) dielectric material not existing as a spacer dielectric
408
Introducing (filling trenches with, polishing) a conductive material
409

FIG. 4A

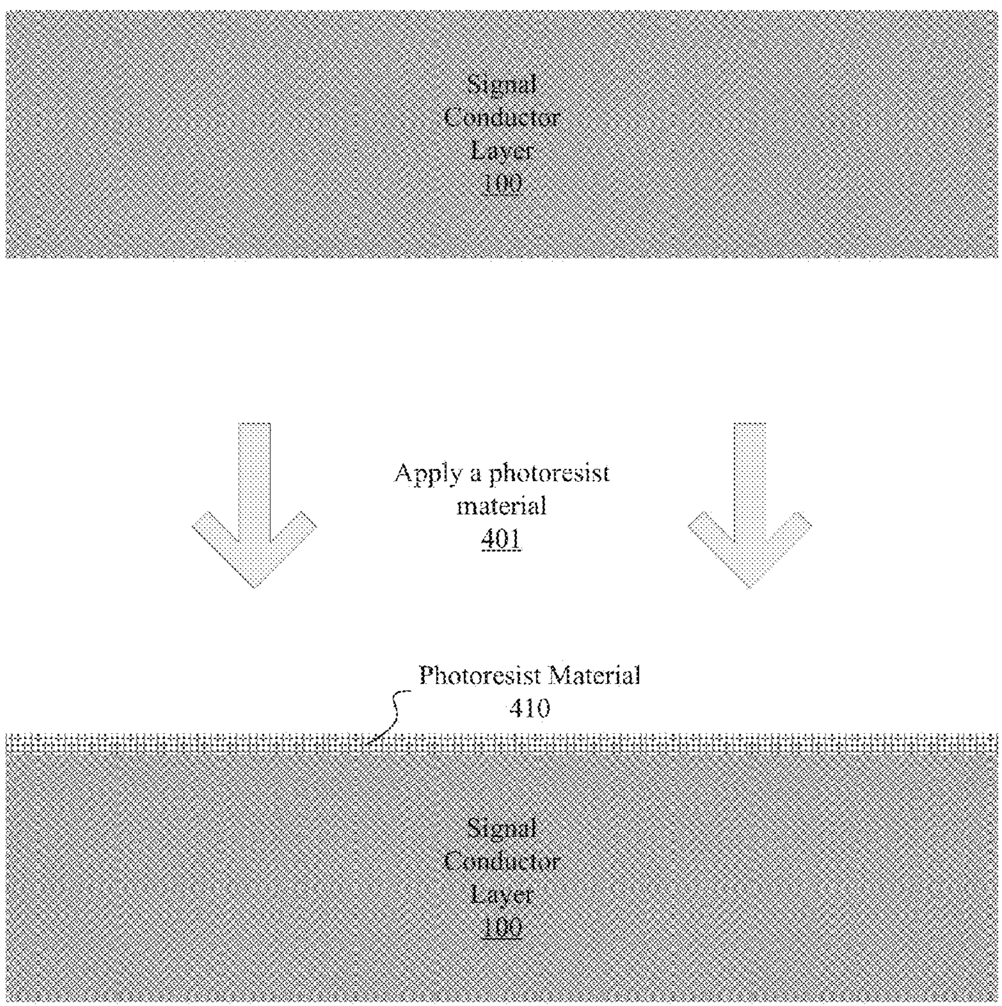
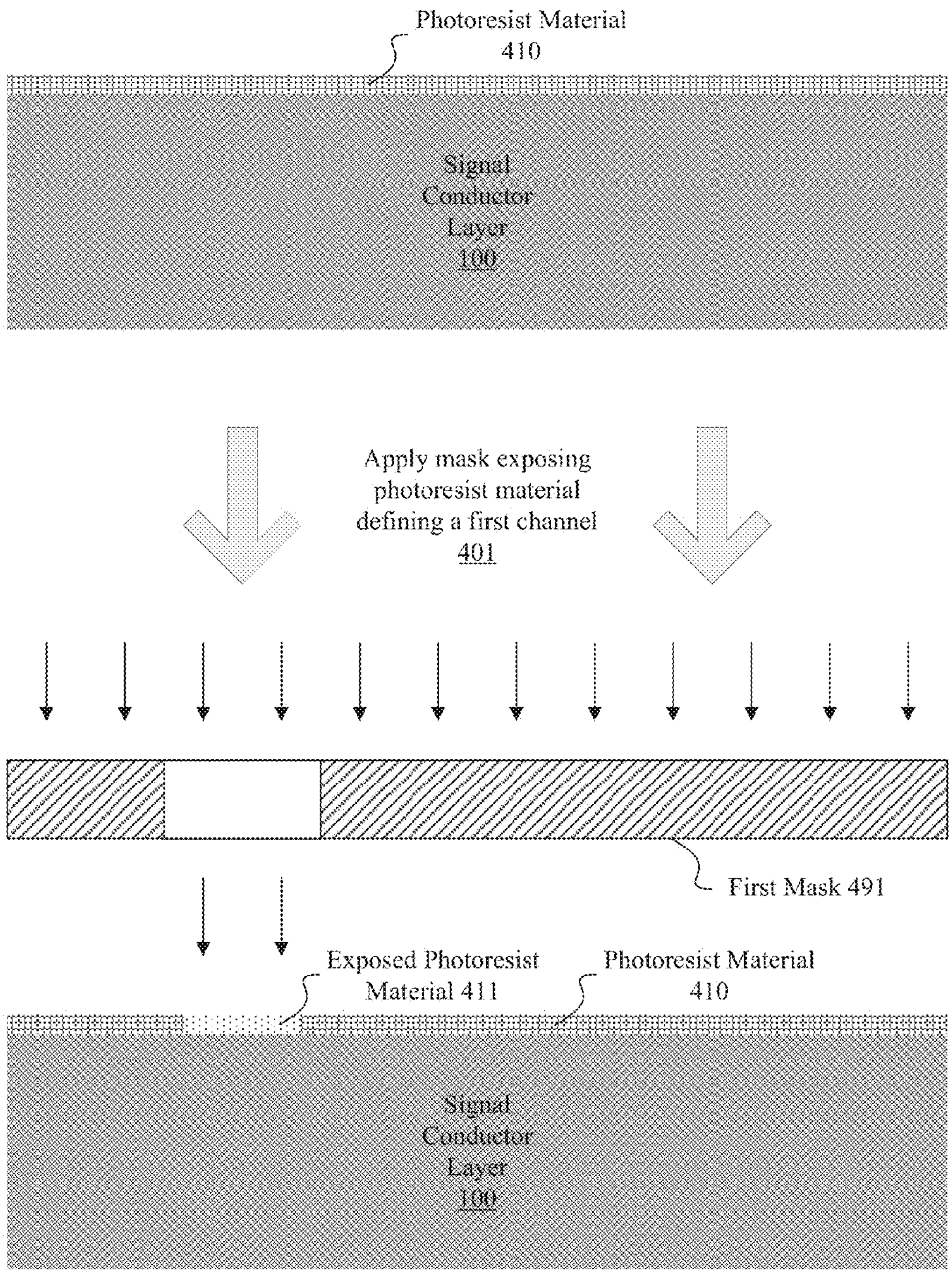

Signal
Conductor
Layer
100
Apply a photoresist
material
401
Photoresist Material
410
Signal
Conductor
Layer
100

FIG. 4B



Photoresist Material
410
Signal
Conductor
Layer
100
Apply mask exposing
photoresist material
defining a first channel
401
First Mask 491
Exposed Photoresist
Material 411
Photoresist Material
410
Signal
Conductor
Layer
100

FIG. 4C

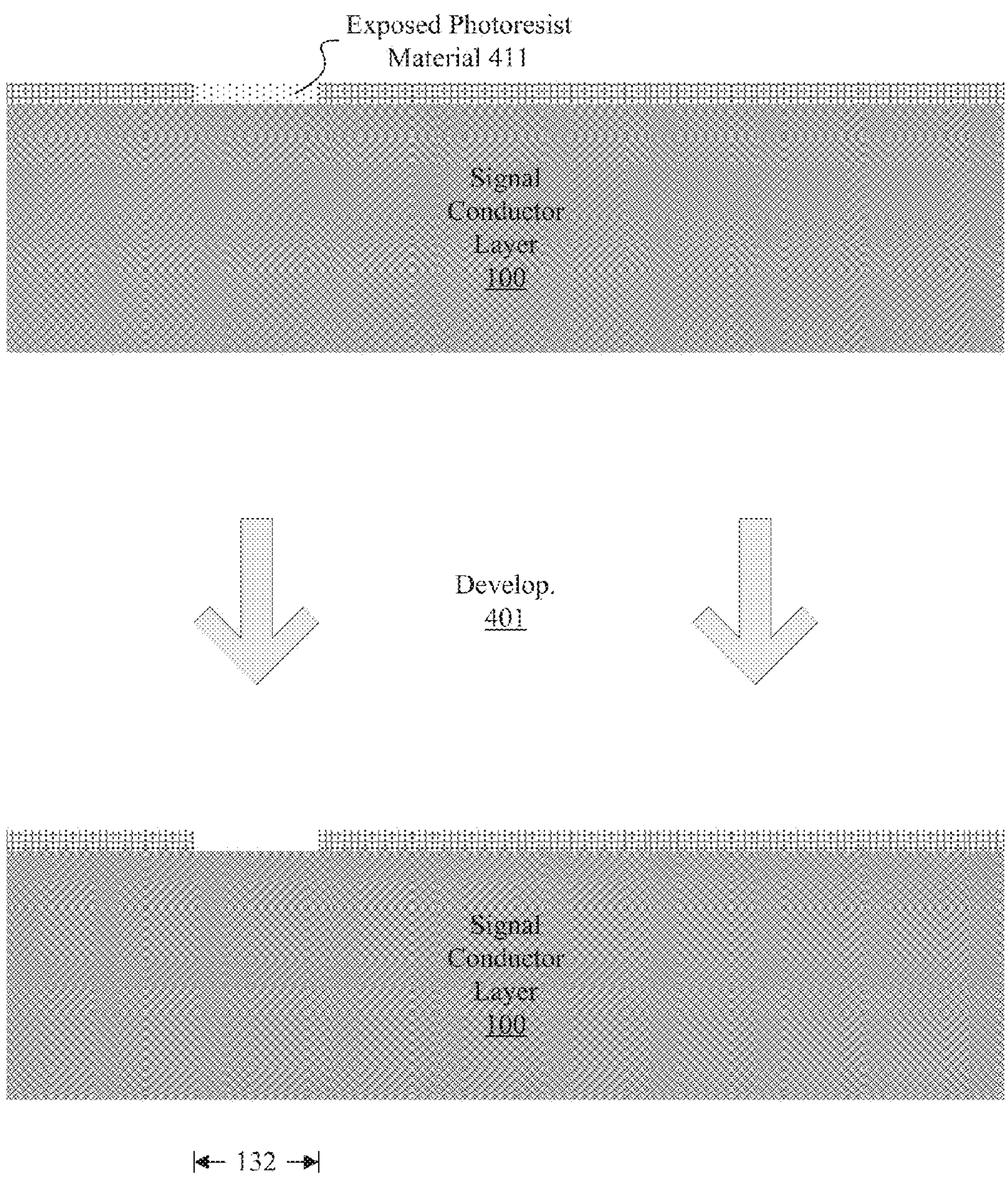

Exposed Photoresist
Material 411
Signal
Conductor
Layer
100
Develop.
401
Signal
Conductor
Layer
100
132

FIG. 4D

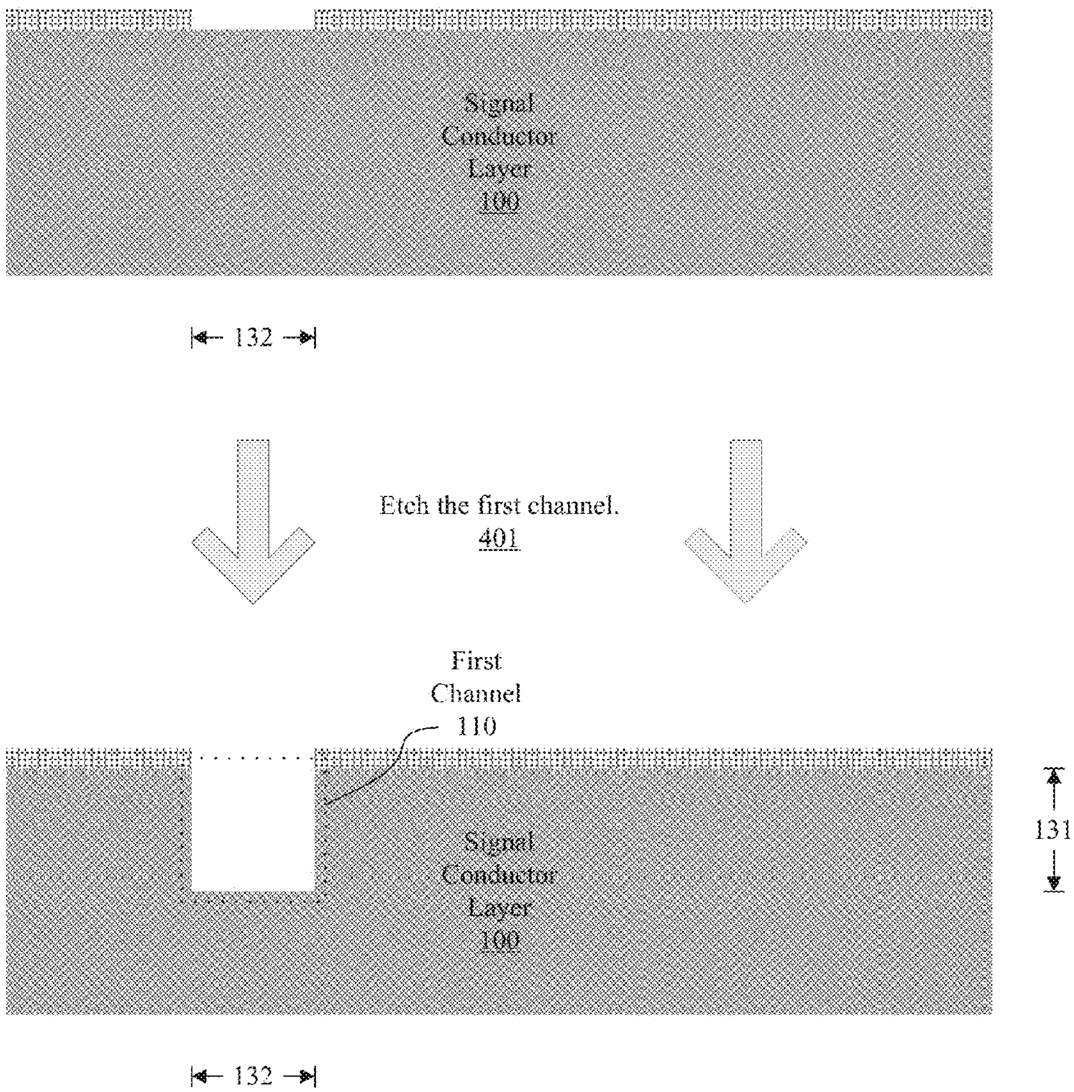

Signal
Conductor
Layer
100
132
Etch the first channel.
401
First
Channel
110
Signal
Conductor
Layer
100
131
132

FIG. 4E

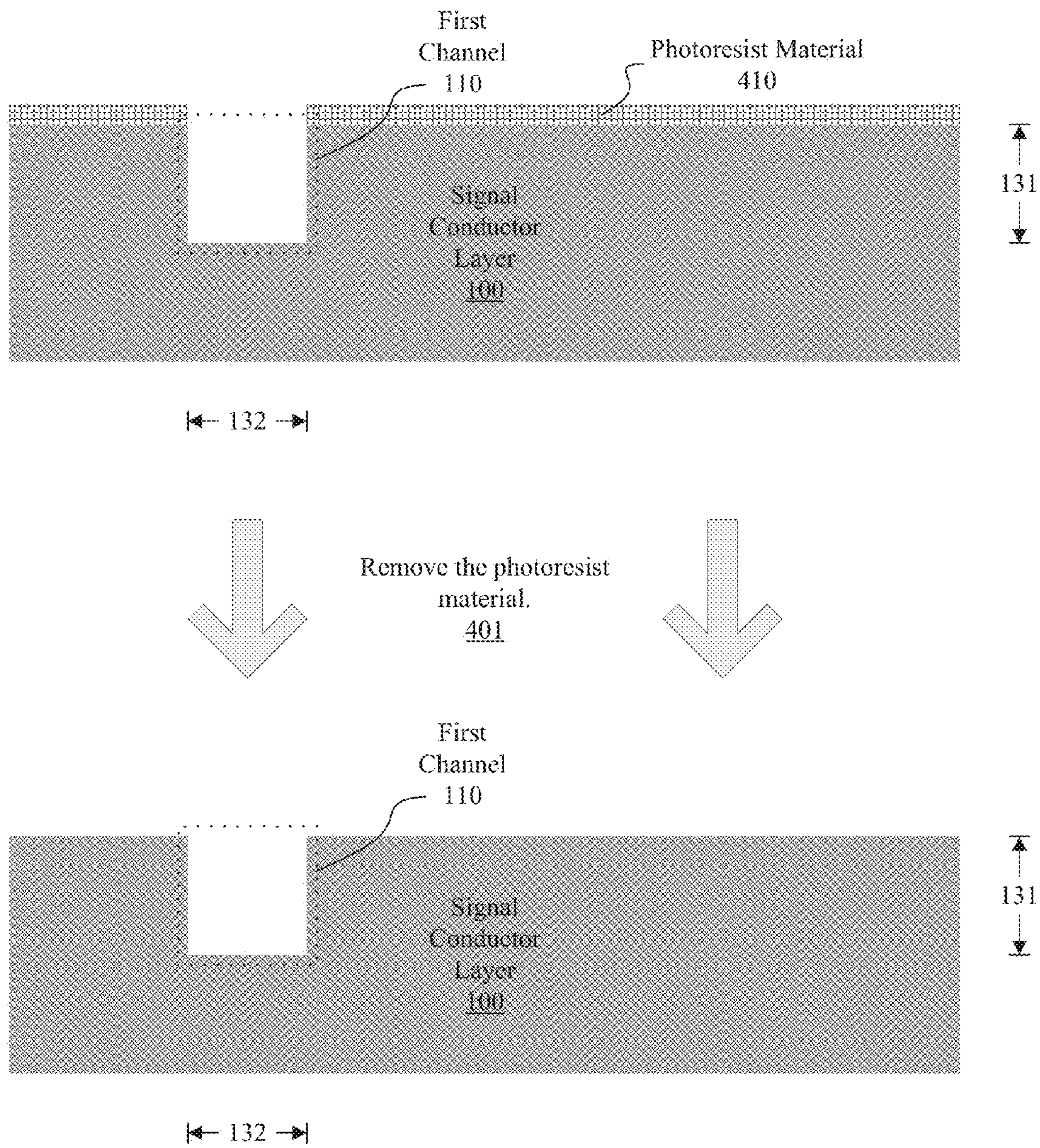

First
Channel
110
Photoresist Material
410
Signal
Conductor
Layer
100
131
132
Remove the photoresist
material.
401
First
Channel
110
Signal
Conductor
Layer
100
131
132

FIG. 4F

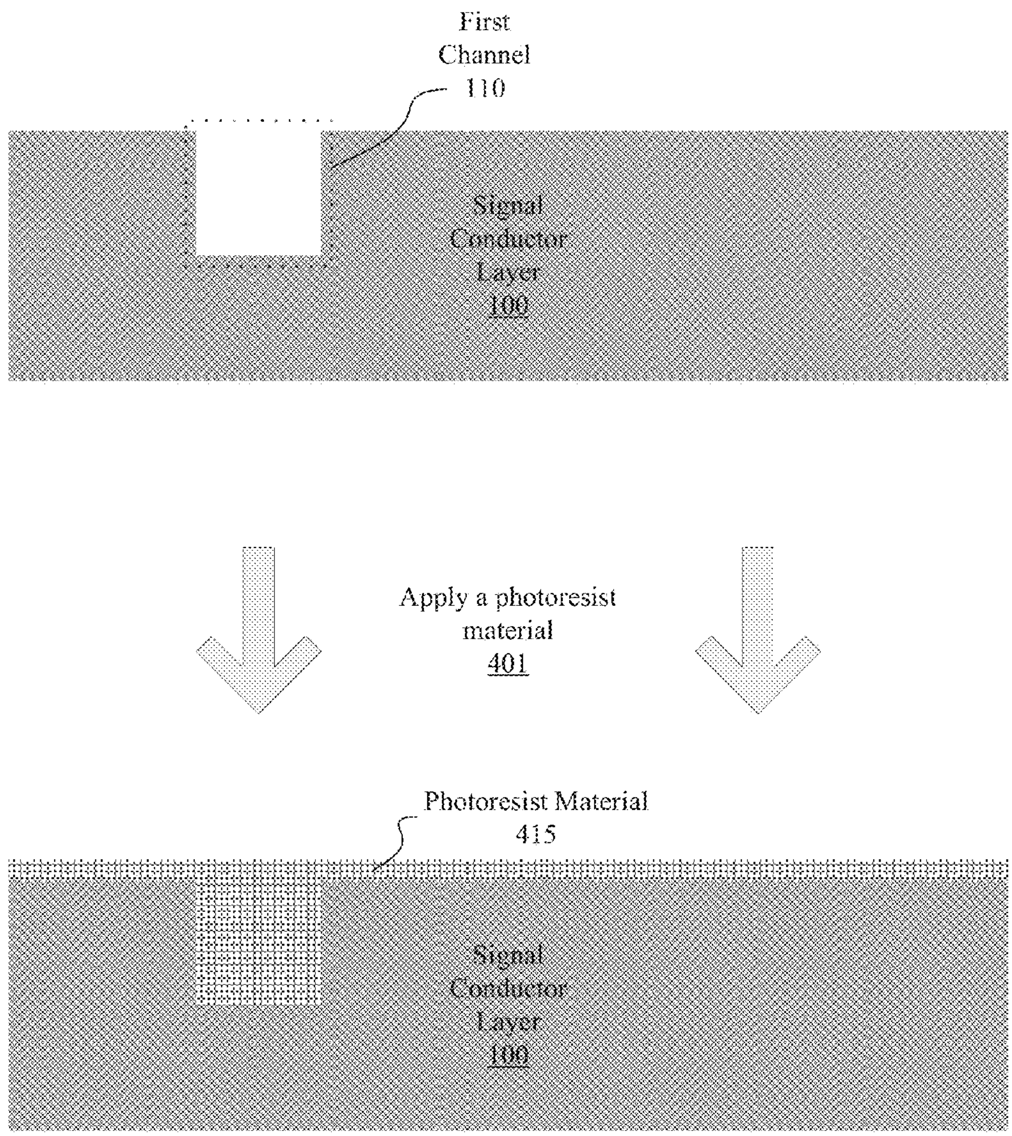

First
Channel
110
Signal
Conductor
Layer
100
Apply a photoresist
material
401
Photoresist Material
415
Signal
Conductor
Layer
100

FIG. 4G

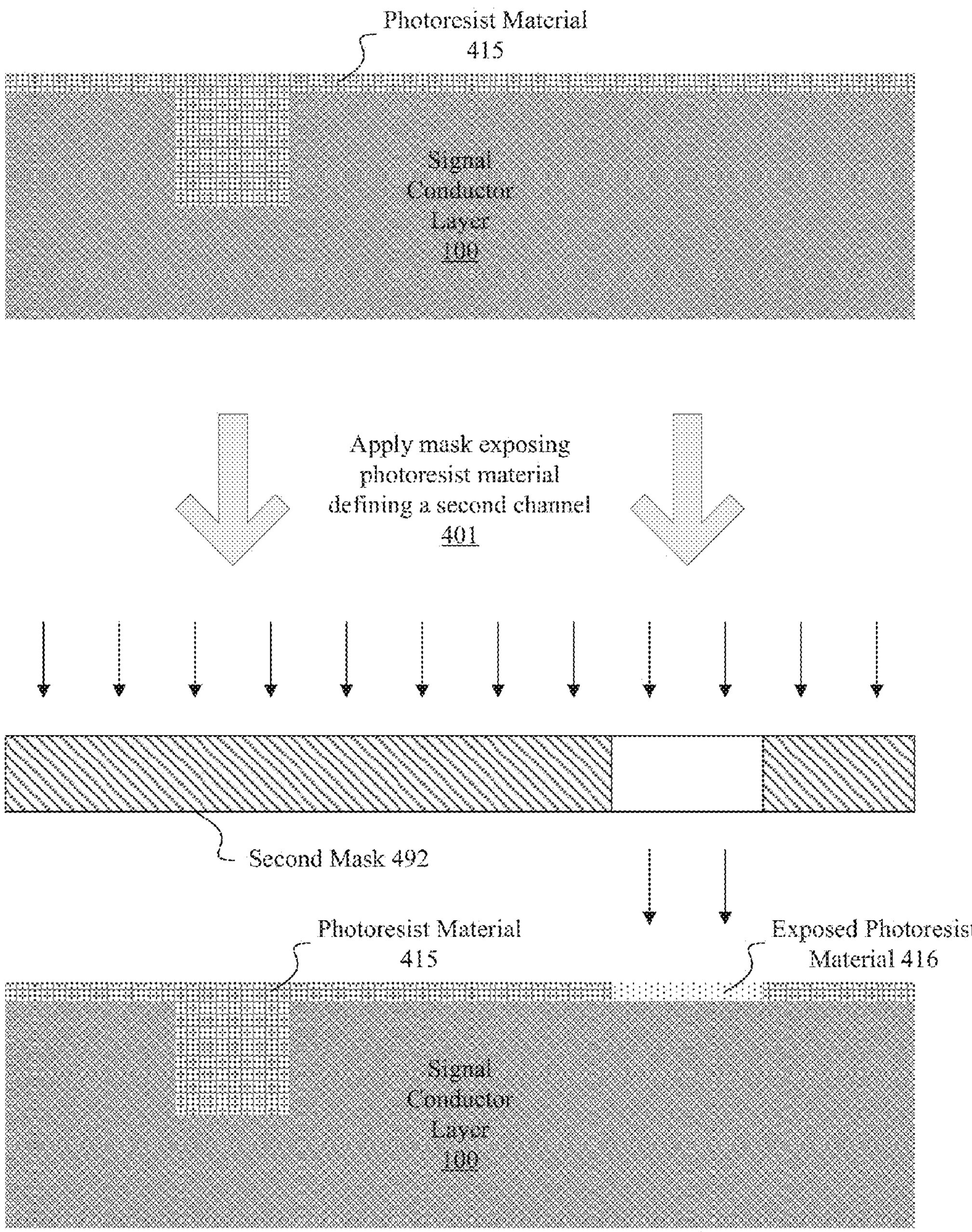

Photoresist Material
415
Signal
Conductor
Layer
100
Apply mask exposing
photoresist material
defining a second channel
401
Second Mask 492
Photoresist Material
415
Exposed Photoresist
Material 416
Signal
Conductor
Layer
100

FIG. 4H

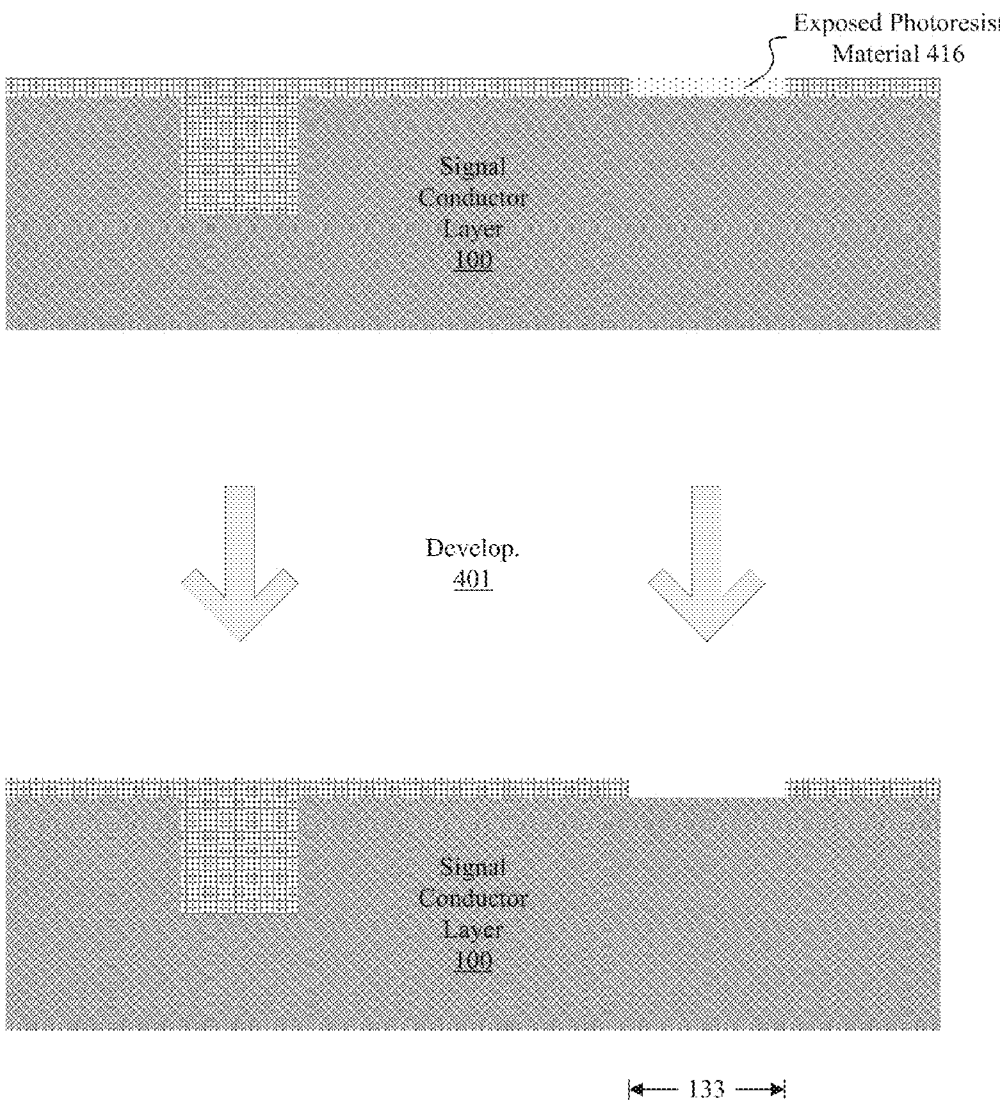

Exposed Photoresist Material 416
Signal Conductor Layer 100
Develop. 401
Signal Conductor Layer 100
133

FIG. 4I

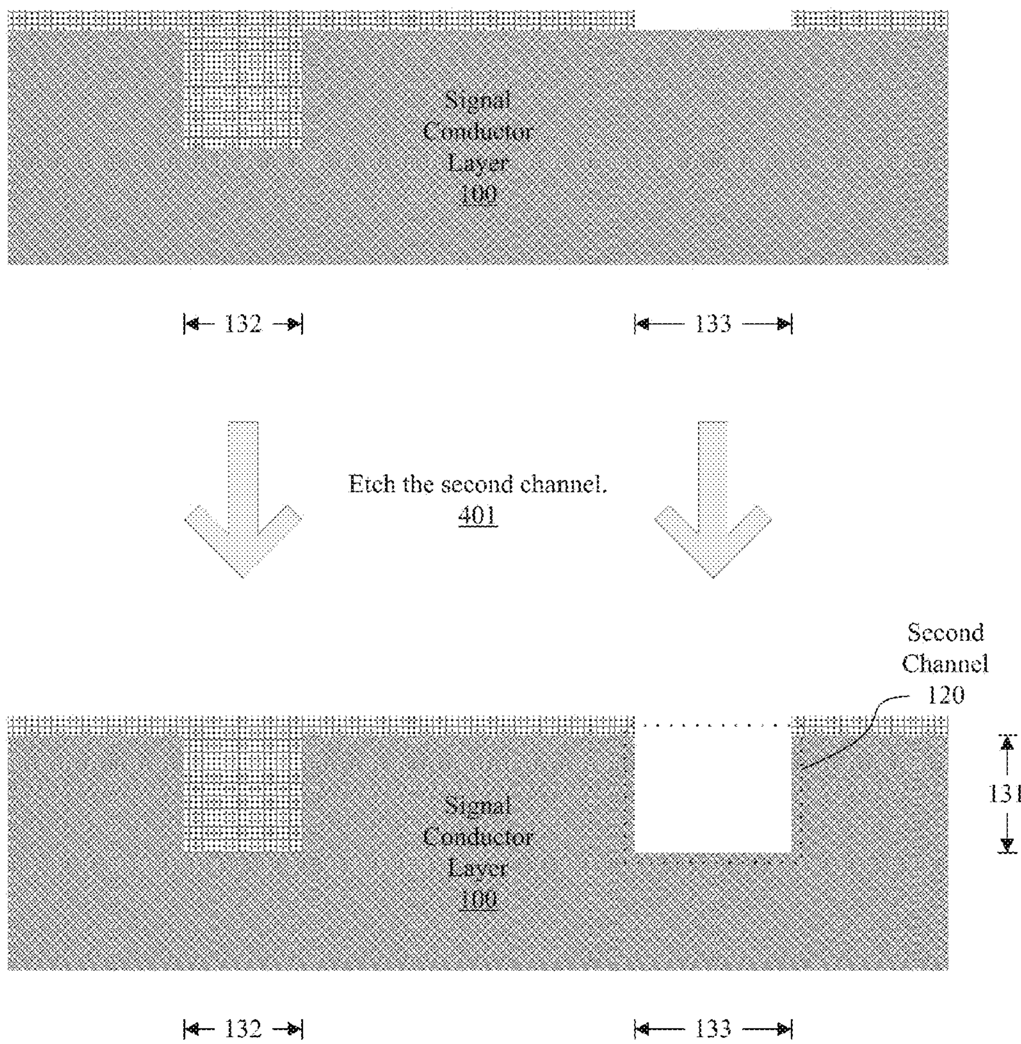

Signal
Conductor
Layer
100
132
133
Etch the second channel.
401
Second
Channel
120
131
Signal
Conductor
Layer
100
132
133

FIG. 4J

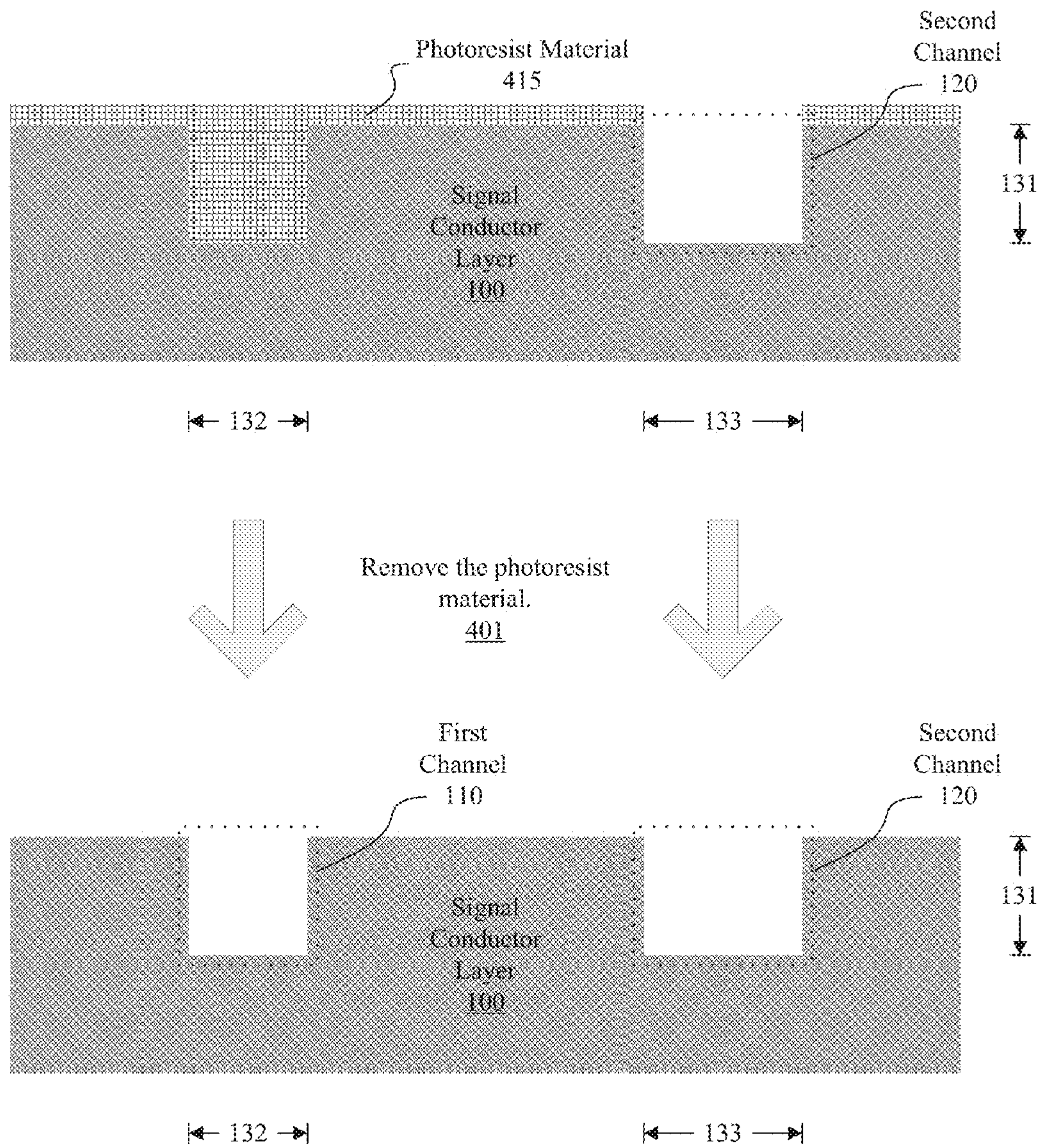

Photoresist Material
415
Second
Channel
120
131
Signal
Conductor
Layer
100
132
133
Remove the photoresist
material.
401
First
Channel
110
Second
Channel
120
131
Signal
Conductor
Layer
100
132
133

FIG. 4K

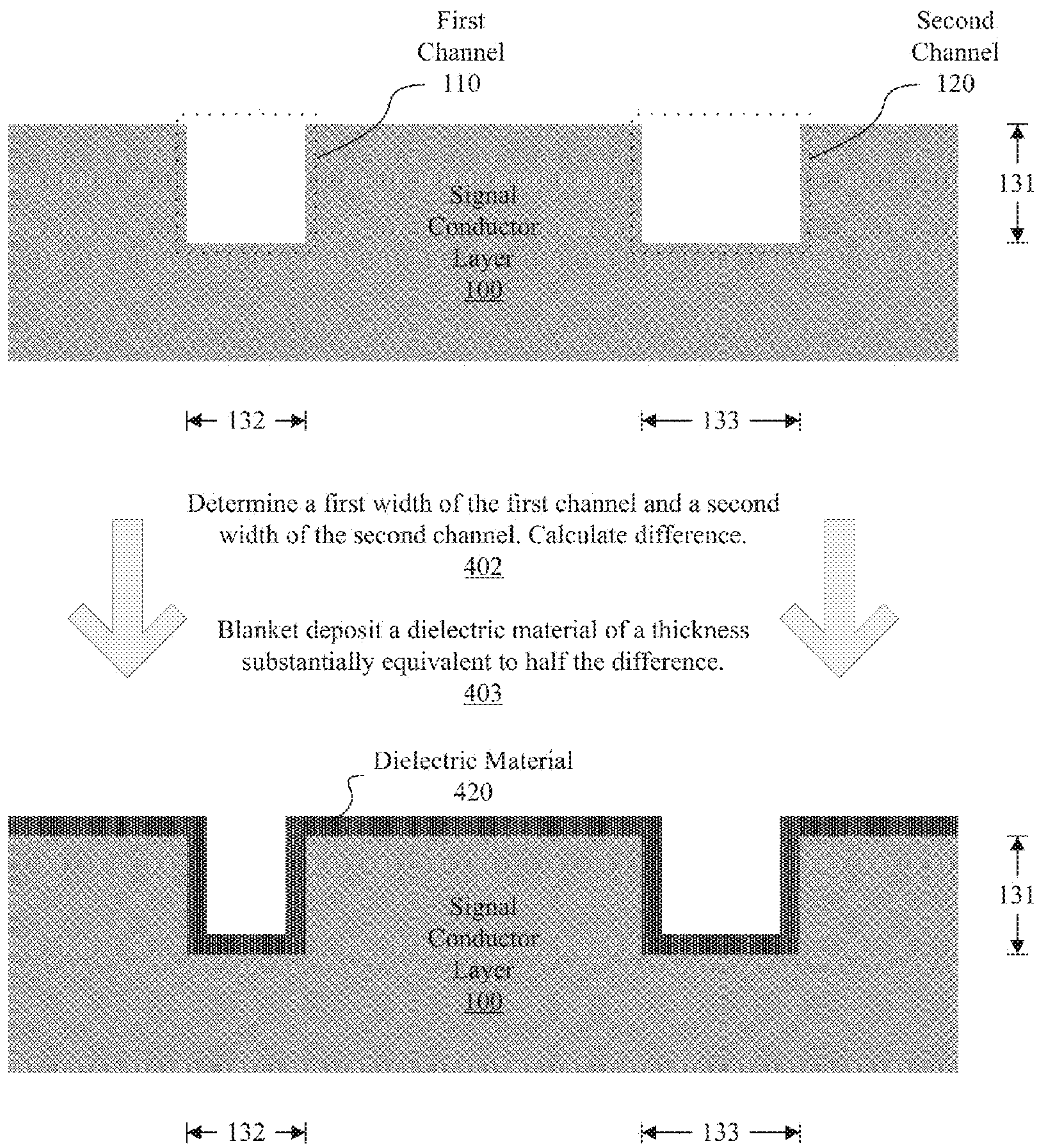

First
Channel
110
Second
Channel
120
131
Signal
Conductor
Layer
100
132
133
Determine a first width of the first channel and a second width of the second channel. Calculate difference.
402
Blanket deposit a dielectric material of a thickness substantially equivalent to half the difference.
403
Dielectric Material
420
131
Signal
Conductor
Layer
100
132
133

FIG. 4L

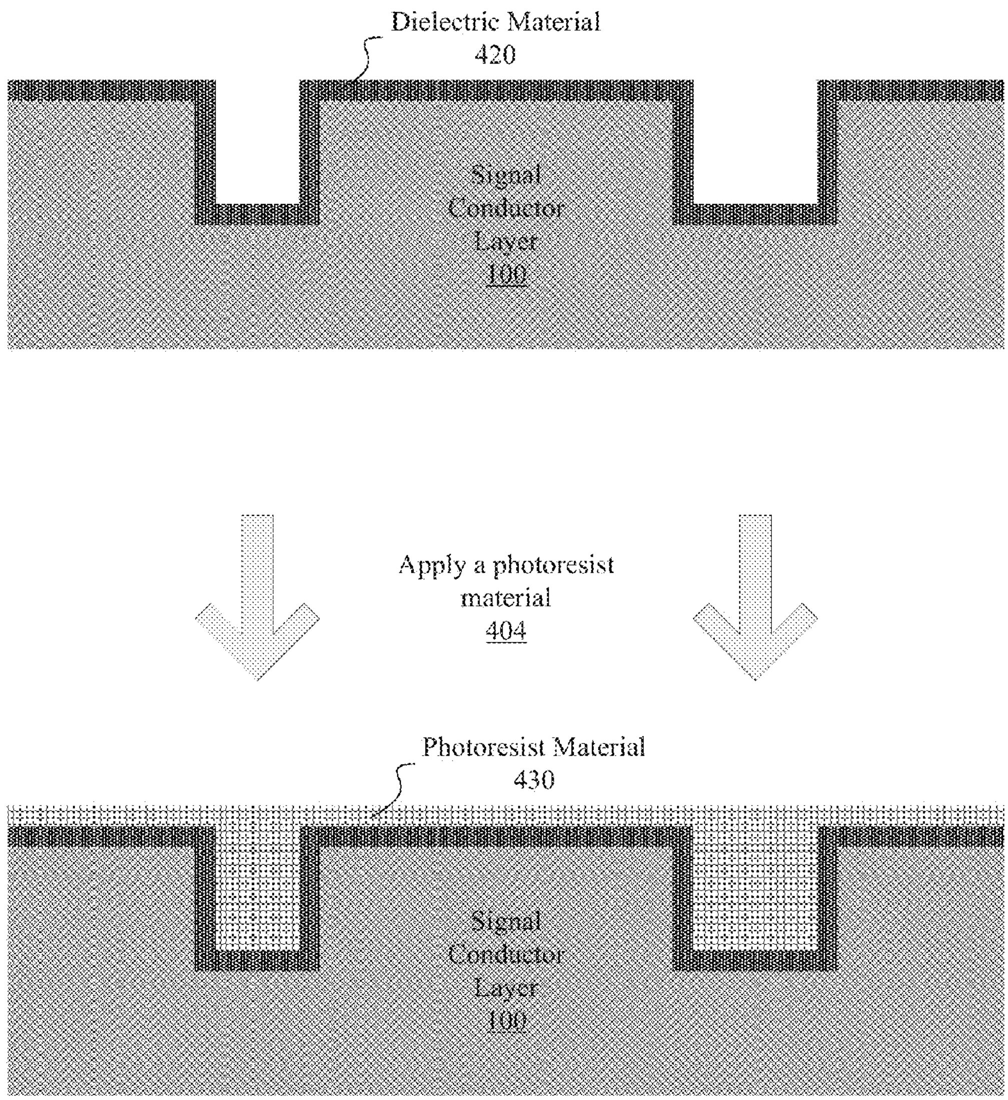

Dielectric Material
420
Signal
Conductor
Layer
100
Apply a photoresist
material
404
Photoresist Material
430
Signal
Conductor
Layer
100

FIG. 4M

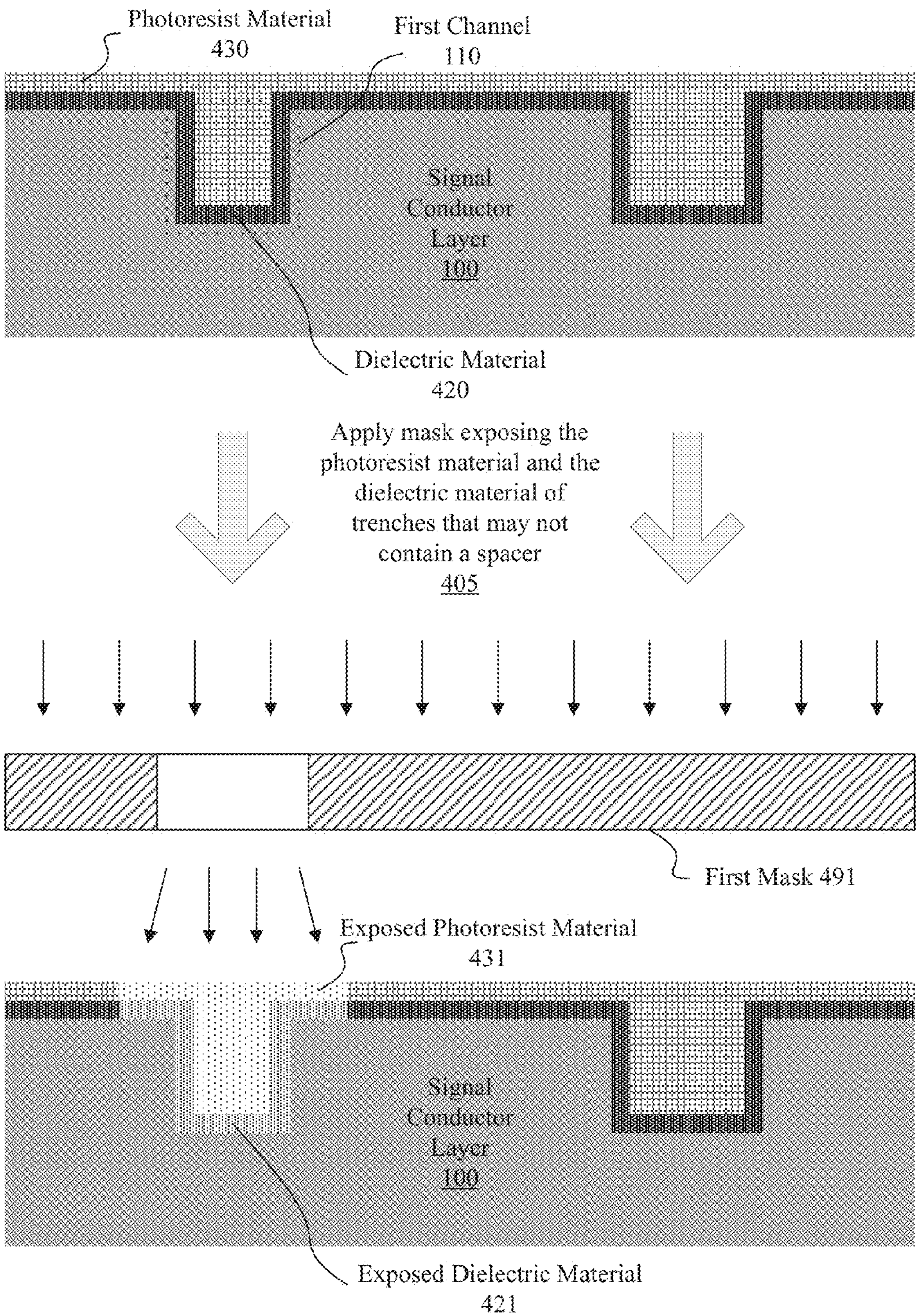

Photoresist Material
430
First Channel
110
Signal
Conductor
Layer
100
Dielectric Material
420
Apply mask exposing the photoresist material and the dielectric material of trenches that may not contain a spacer
405
First Mask 491
Exposed Photoresist Material
431
Signal
Conductor
Layer
100
Exposed Dielectric Material
421

FIG. 4N

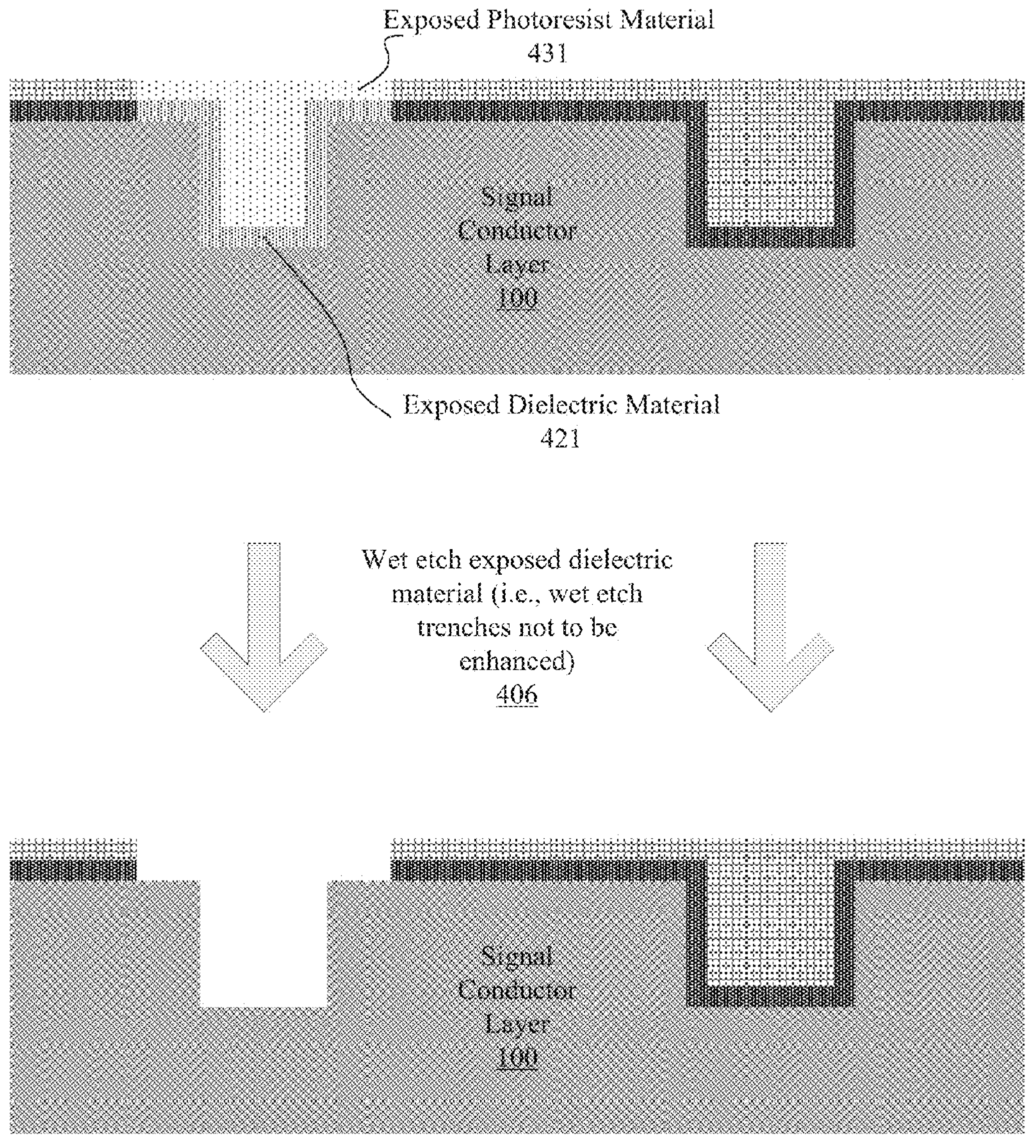

Exposed Photoresist Material
431
Signal
Conductor
Layer
100
Exposed Dielectric Material
421
Wet etch exposed dielectric
material (i.e., wet etch
trenches not to be
enhanced)
406
Signal
Conductor
Layer
100

FIG. 4O

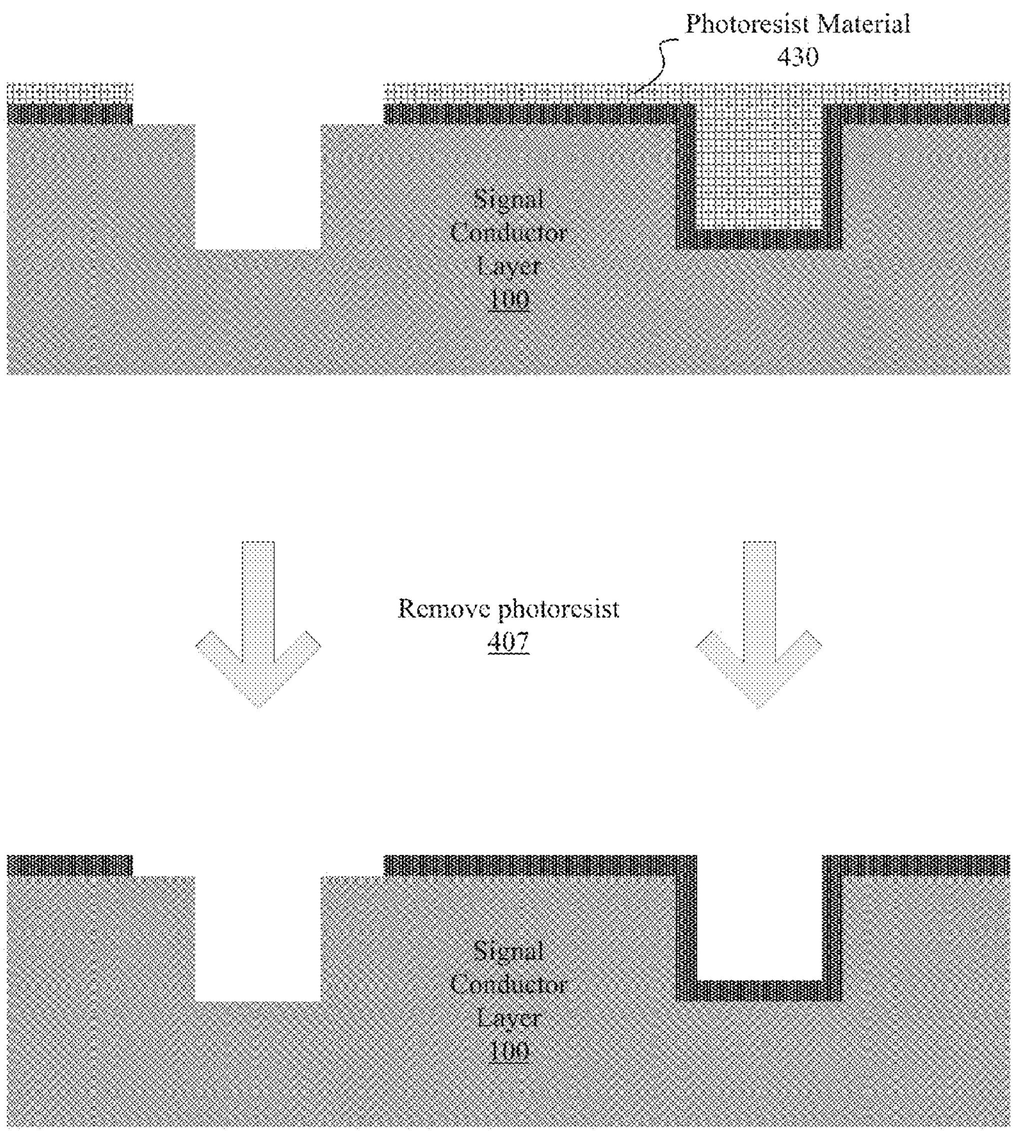

Photoresist Material
430
Signal
Conductor
Layer
100
Remove photoresist
407
Signal
Conductor
Layer
100

FIG. 4P

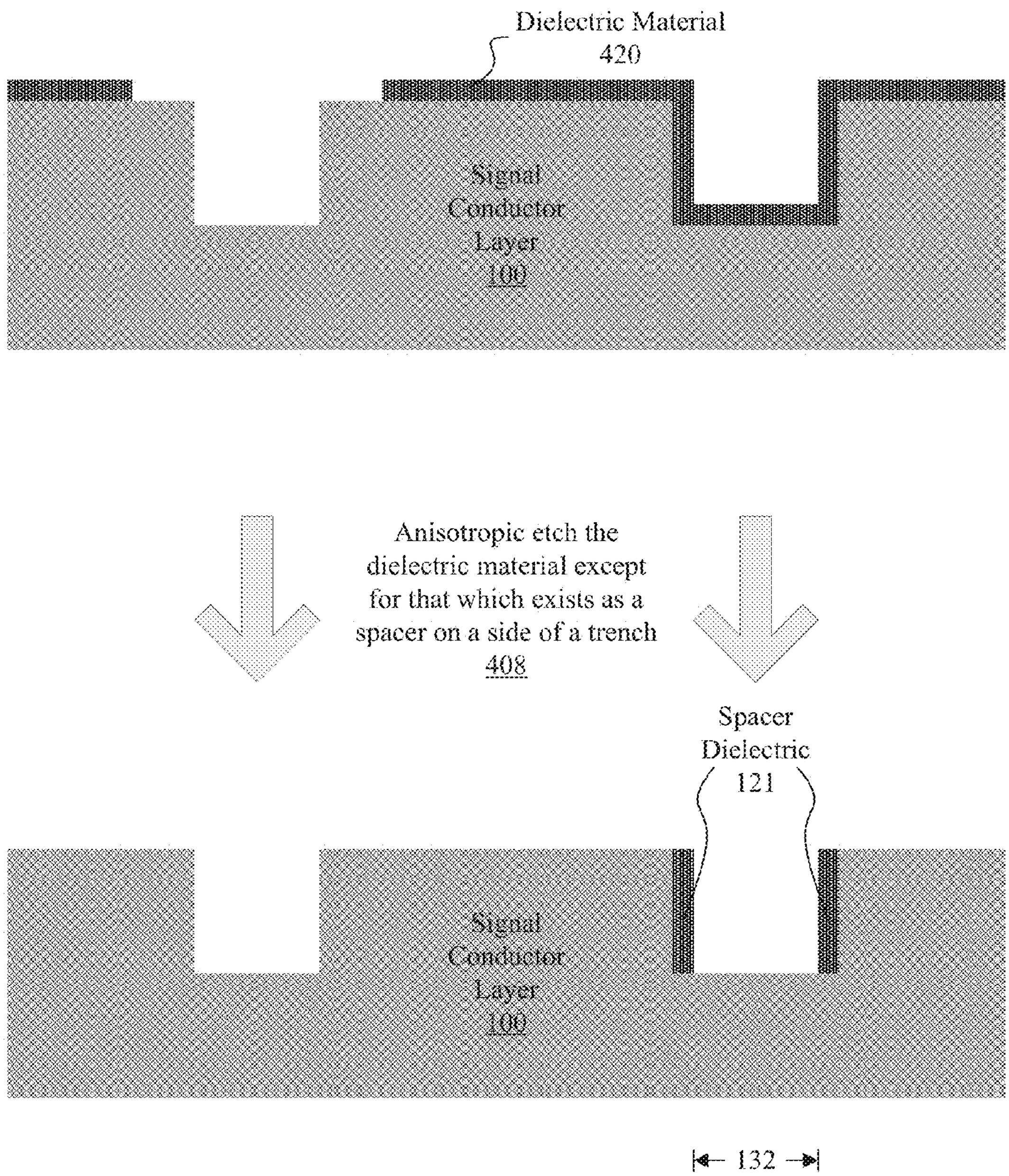
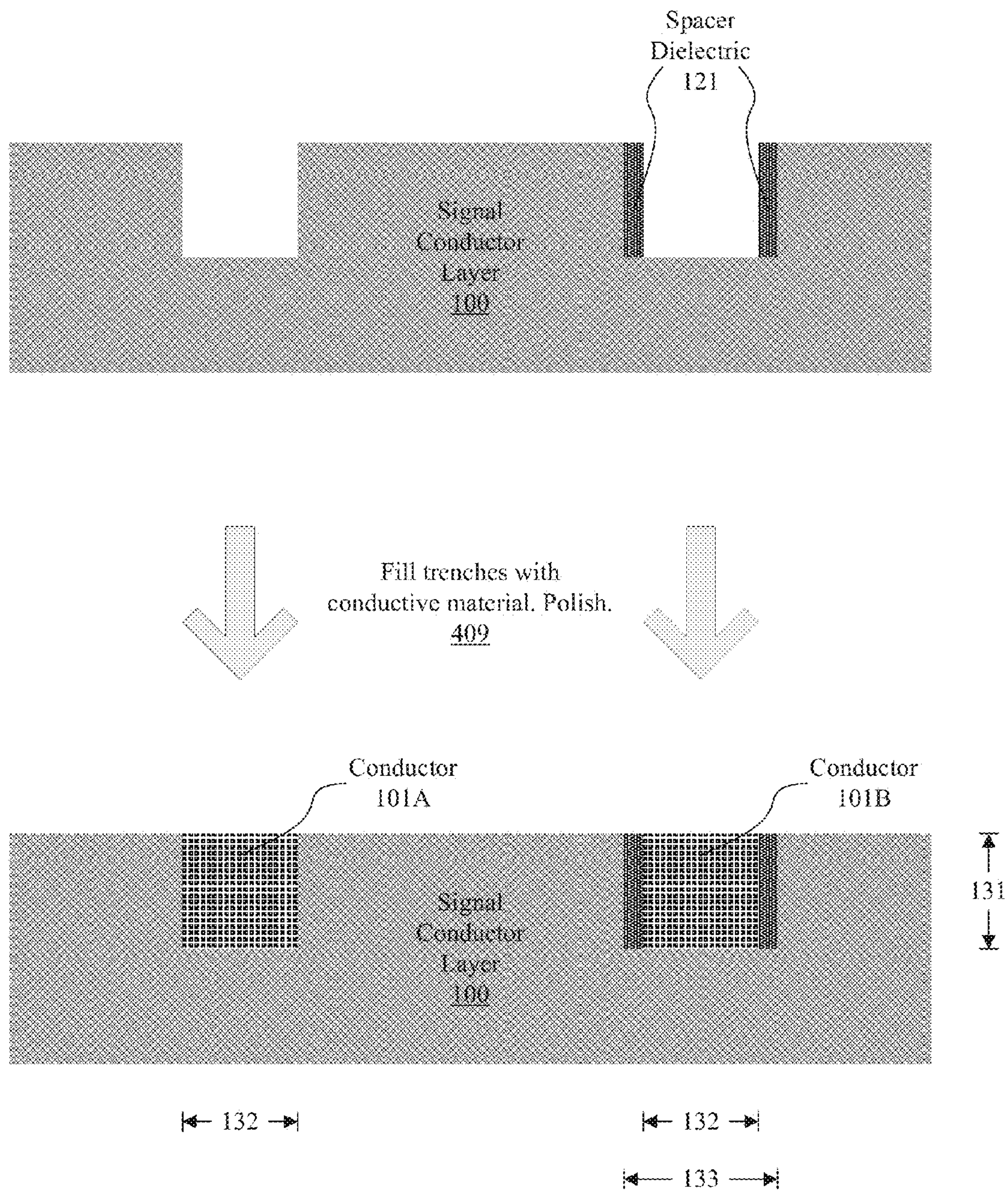

Dielectric Material
420
Signal
Conductor
Layer
100
Anisotropic etch the
dielectric material except
for that which exists as a
spacer on a side of a trench
408
Spacer
Dielectric
121
Signal
Conductor
Layer
100
132

FIG. 4Q



Spacer
Dielectric
121
Signal
Conductor
Layer
100
Fill trenches with
conductive material. Polish.
409
Conductor
101A
Conductor
101B
Signal
Conductor
Layer
100
131
132
132
133

FIG. 4R

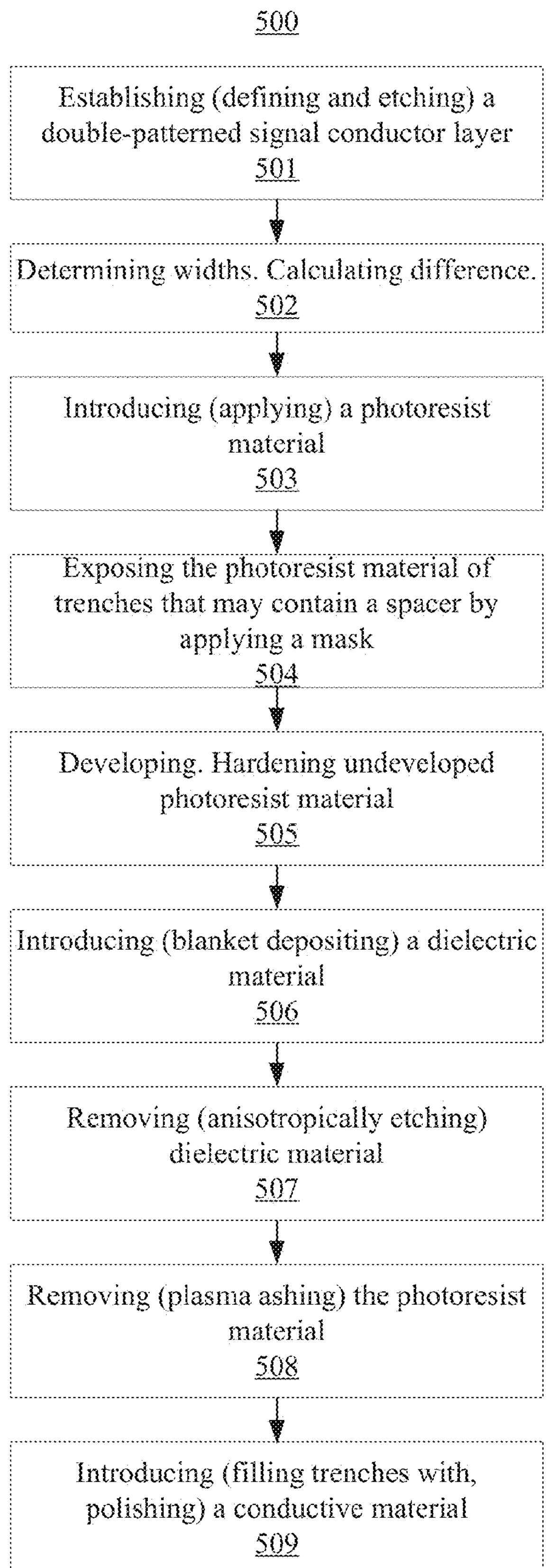

500
Establishing (defining and etching) a double-patterned signal conductor layer
501
Determining widths. Calculating difference.
502
Introducing (applying) a photoresist material
503
Exposing the photoresist material of trenches that may contain a spacer by applying a mask
504
Developing. Hardening undeveloped photoresist material
505
Introducing (blanket depositing) a dielectric material
506
Removing (anisotropically etching) dielectric material
507
Removing (plasma ashing) the photoresist material
508
Introducing (filling trenches with, polishing) a conductive material
509

FIG. 5A

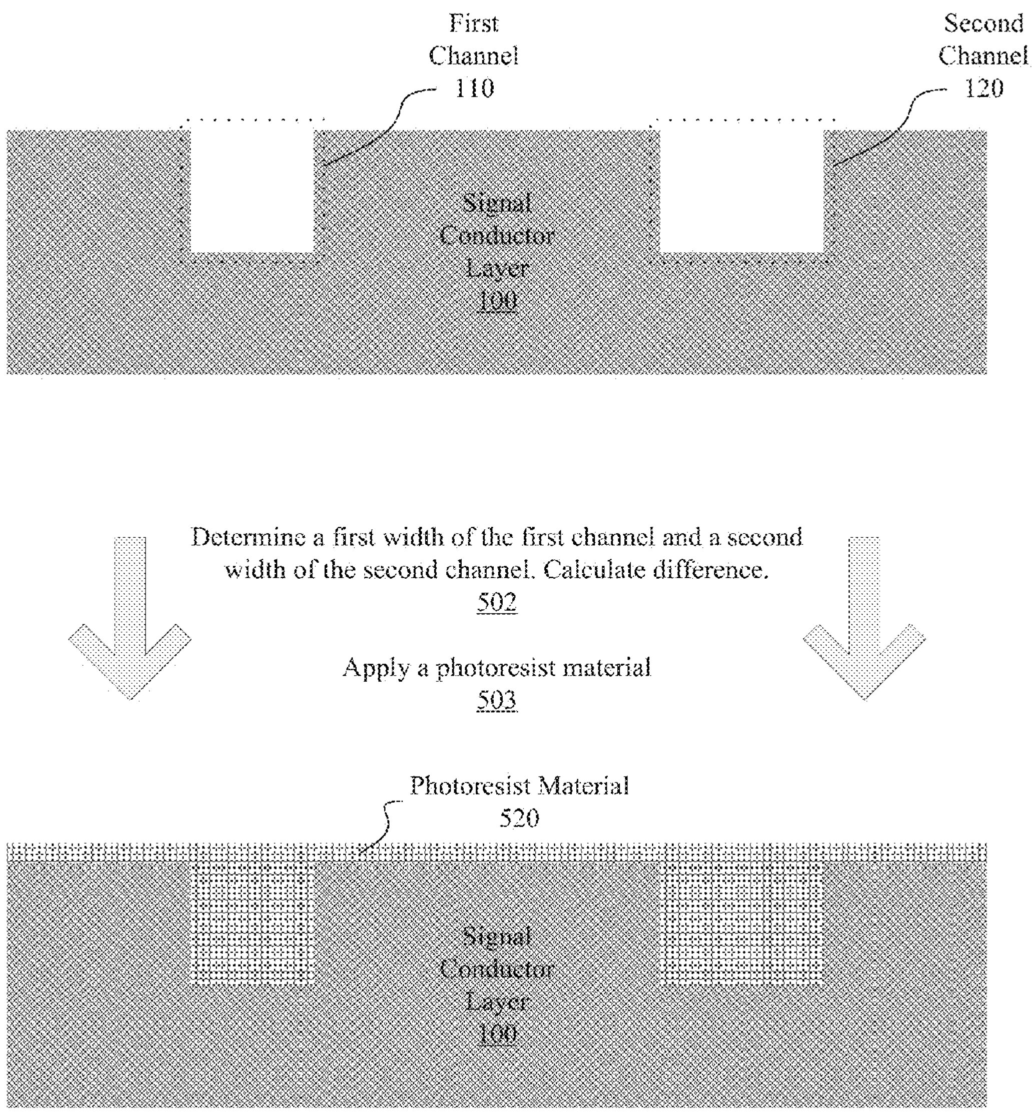

First Channel 110
Second Channel 120
Signal Conductor Layer 100
Determine a first width of the first channel and a second width of the second channel. Calculate difference. 502
Apply a photoresist material 503
Photoresist Material 520
Signal Conductor Layer 100

FIG. 5B

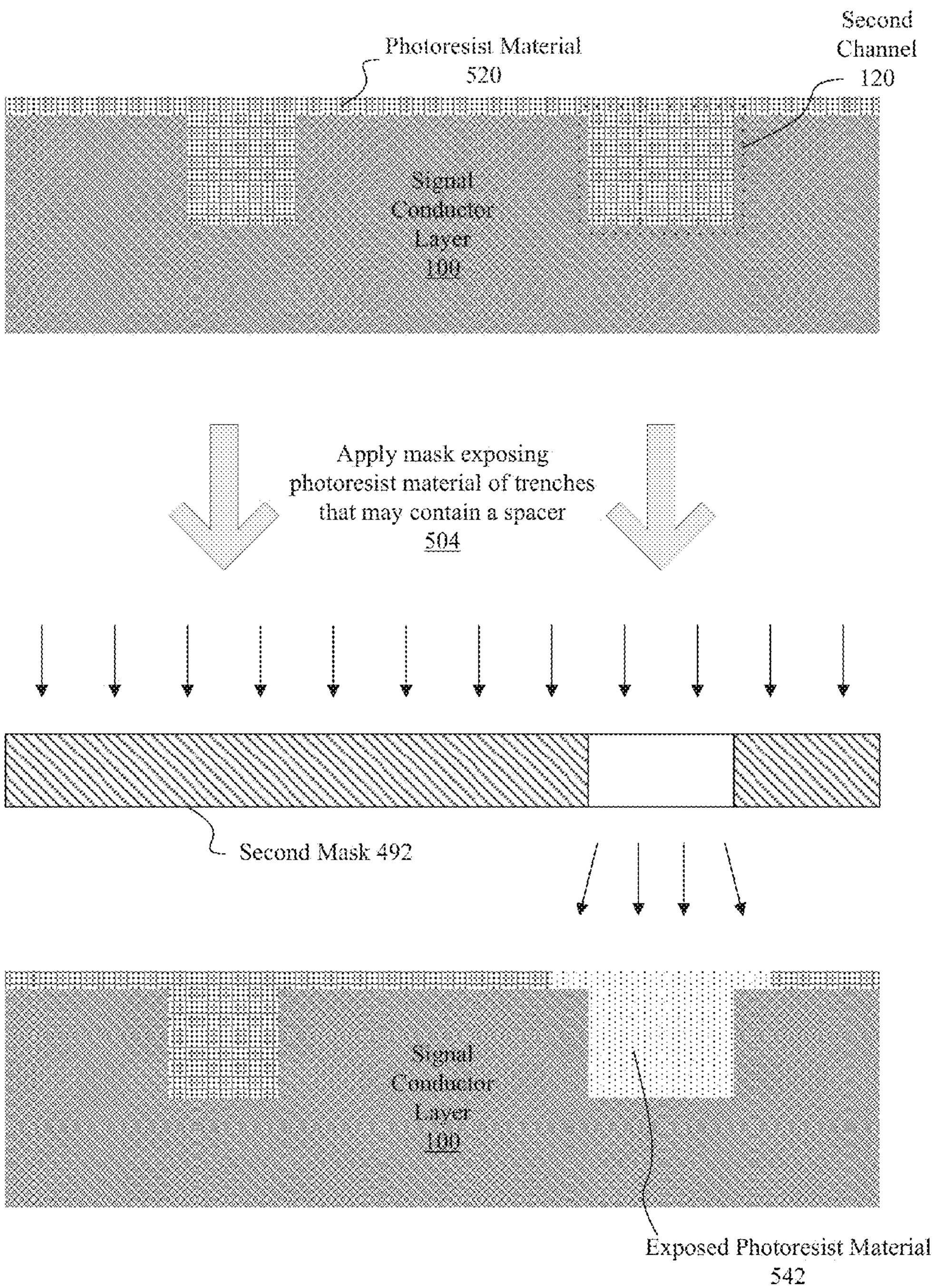

Photoresist Material
520
Second
Channel
120
Signal
Conductor
Layer
100
Apply mask exposing
photoresist material of trenches
that may contain a spacer
504
Second Mask 492
Signal
Conductor
Layer
100
Exposed Photoresist Material
542

FIG. 5C

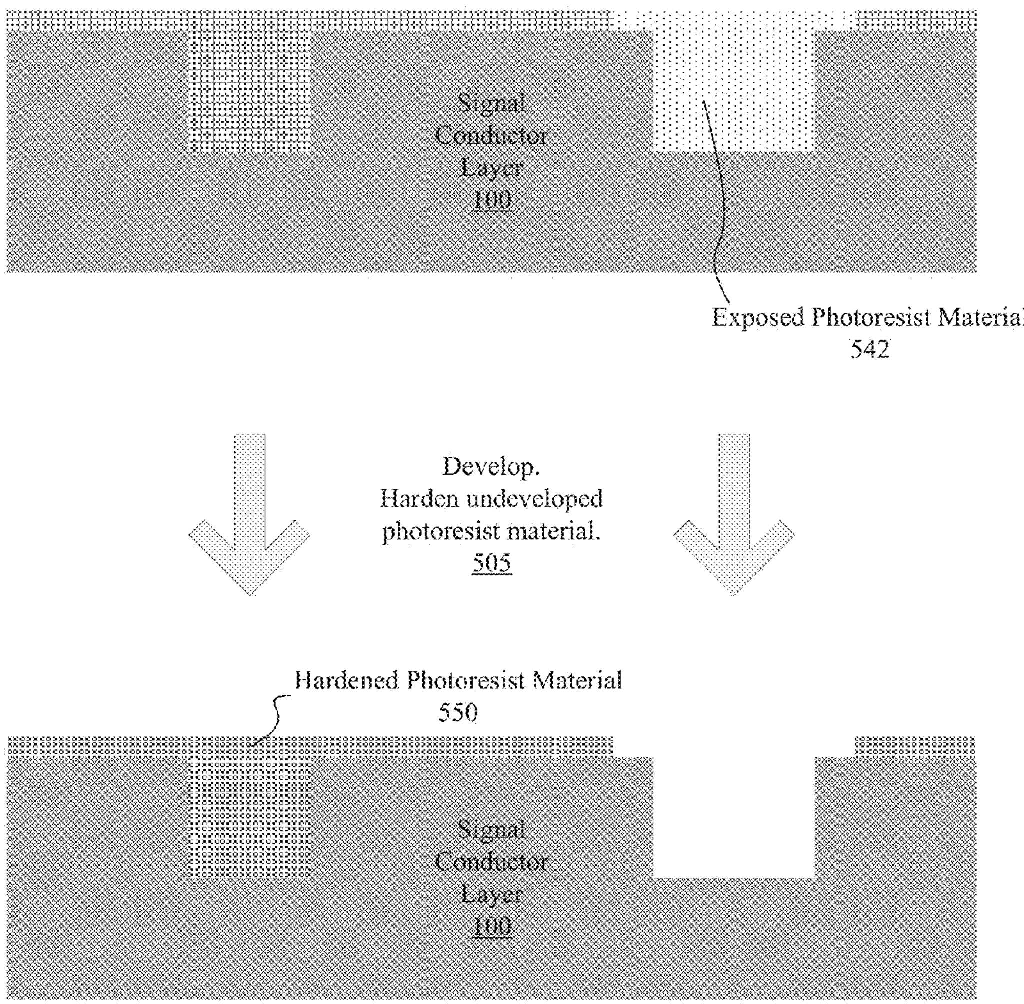

Signal
Conductor
Layer
100
Exposed Photoresist Material
542
Develop.
Harden undeveloped
photoresist material.
505
Hardened Photoresist Material
550
Signal
Conductor
Layer
100

FIG. 5D

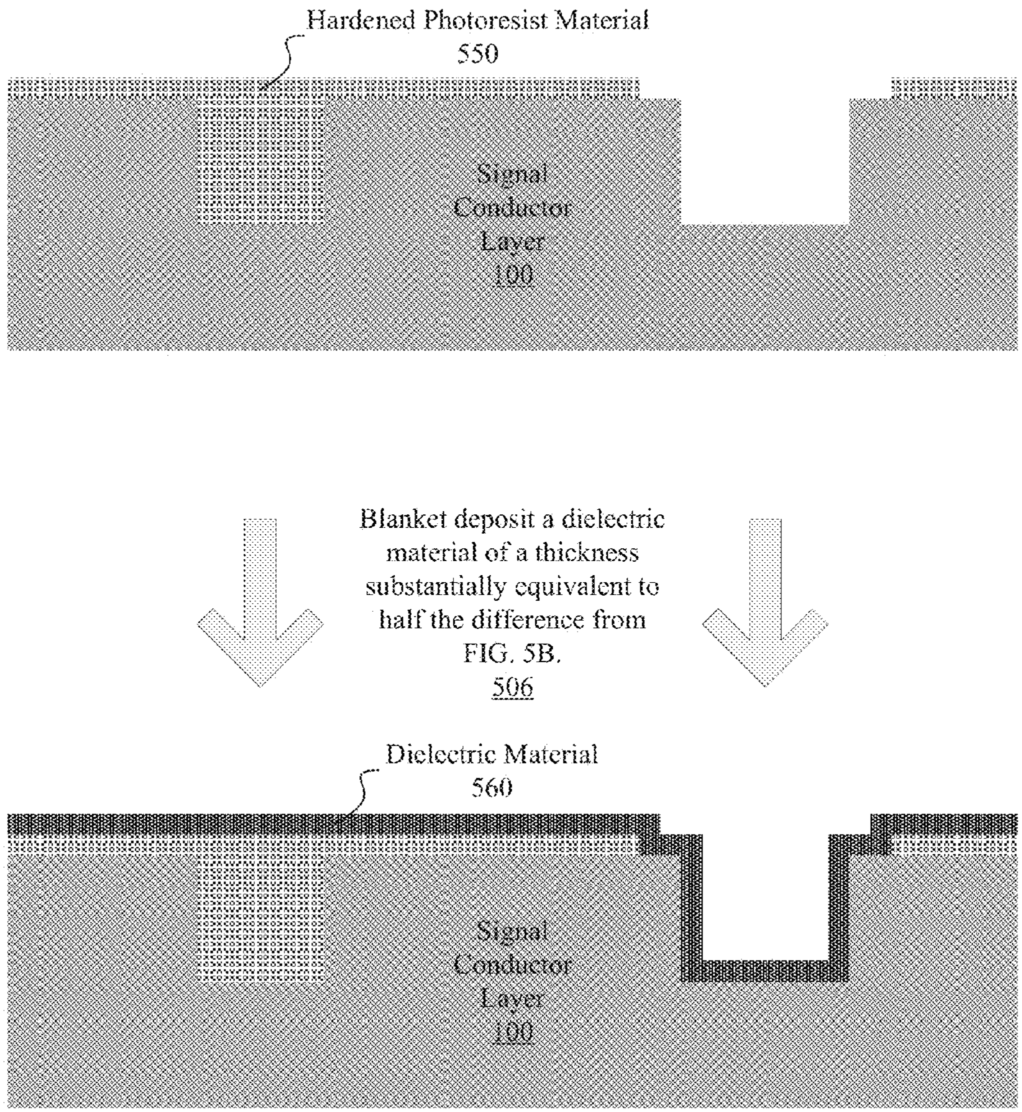
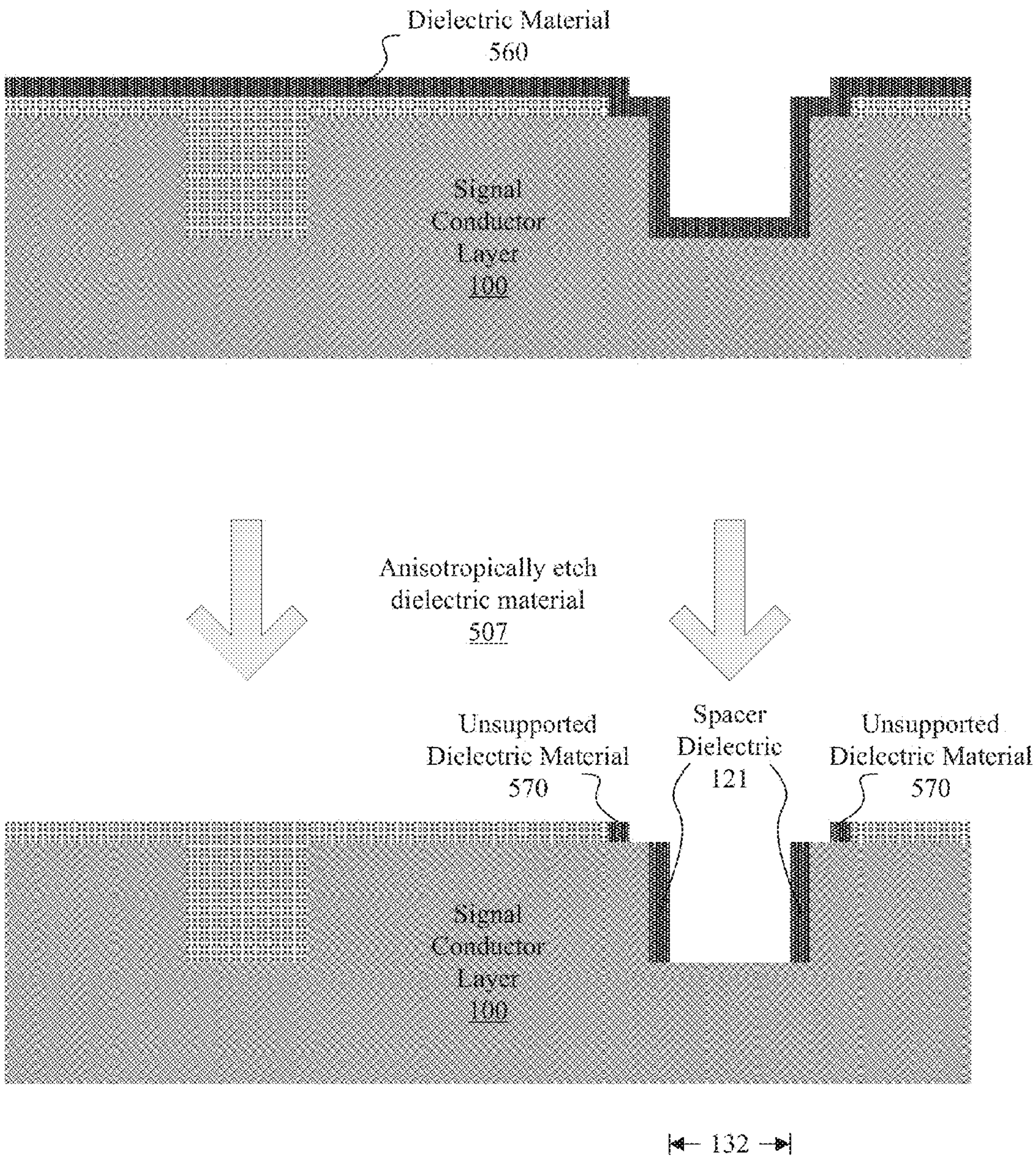

Hardened Photoresist Material
550
Signal
Conductor
Layer
100
Blanket deposit a dielectric
material of a thickness
substantially equivalent to
half the difference from
FIG. 5B.
506
Dielectric Material
560
Signal
Conductor
Layer
100

FIG. 5E



Dielectric Material
560
Signal
Conductor
Layer
100
Anisotropically etch
dielectric material
507
Unsupported
Dielectric Material
570
Spacer
Dielectric
121
Unsupported
Dielectric Material
570
Signal
Conductor
Layer
100
132

FIG. 5F

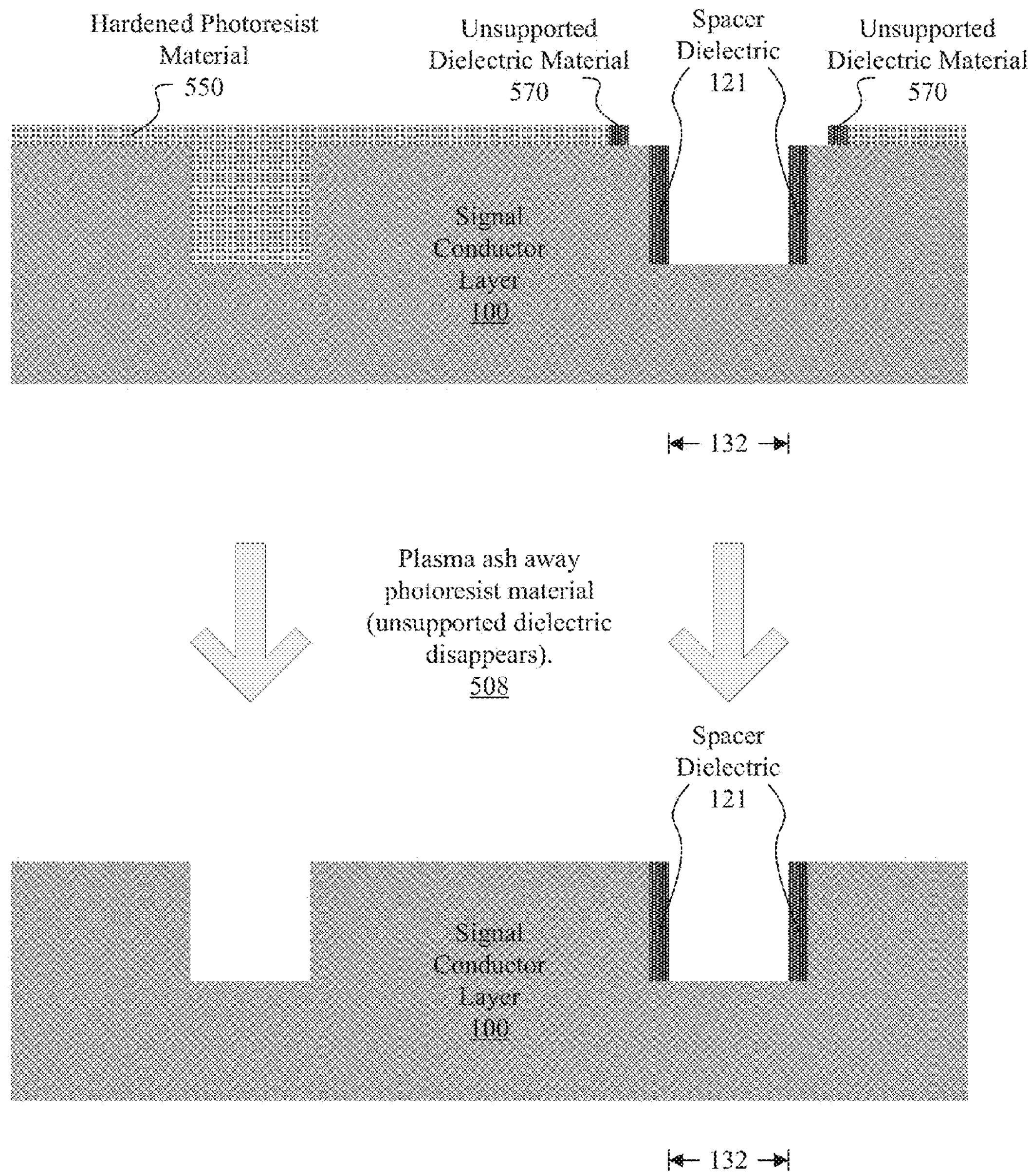

Hardened Photoresist Material 550
Unsupported Dielectric Material 570
Spacer Dielectric 121
Unsupported Dielectric Material 570
Signal Conductor Layer 100
132
Plasma ash away photoresist material (unsupported dielectric disappears). 508
Spacer Dielectric 121
Signal Conductor Layer 100
132

FIG. 5G

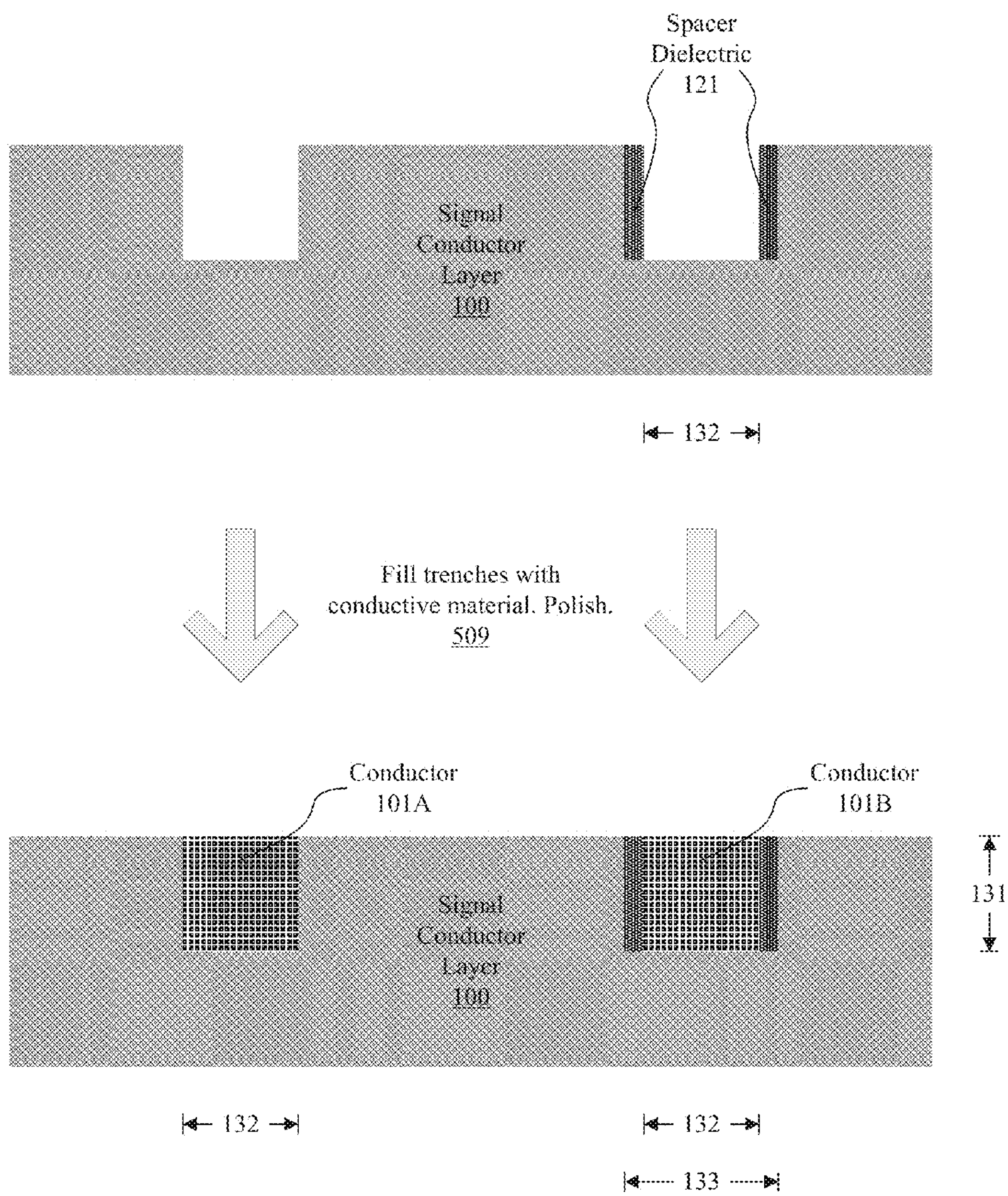

Spacer
Dielectric
121
Signal
Conductor
Layer
100
132
Fill trenches with
conductive material. Polish.
509
Conductor
101A
Conductor
101B
Signal
Conductor
Layer
100
131
132
132
133

FIG. 5H

MULTIPLE-PATTERNED SEMICONDUCTOR DEVICE CHANNELS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of co-pending U.S. patent application Ser. No. 13/795,890 filed Mar. 12, 2013. The aforementioned related patent application is herein incorporated by reference in its entirety.

TECHNICAL FIELD

This disclosure relates generally to a semiconductor device and, more particularly, relates to a multiple-patterned semiconductor device.

BACKGROUND

The semiconductor industry is producing more and more capable components with smaller and smaller feature sizes. The production of such semiconductor devices reveals new design and manufacturing challenges to be addressed in order to maintain or improve semiconductor device performance. Simultaneously having semiconductor wiring stacks with high density, high yield, good signal integrity as well as suitable power delivery may present challenges.

As the device density of semiconductors increases, the conductor line width and spacing within the semiconductor devices decreases. Multiple-pattern lithography represents a class of technologies developed for photolithography to enhance the feature density of semiconductor devices. Double-patterning, a subset of multiple-patterning employs multiple masks and photolithographic steps to create a particular level of a semiconductor device. With benefits such as tighter pitches and narrower wires, double-patterning alters relationships between variables related to semiconductor device wiring and wire quality to sustain performance.

SUMMARY

In an embodiment, this disclosure relates to a semiconductor device. The semiconductor device may include one or more layers. The semiconductor device may be multiple-patterned on a particular level. The semiconductor device may include channels. The channels may be defined by masks. In particular, the semiconductor device may include a first channel defined by a first mask and a second channel defined by a second mask. The first channel may have a first width and the second channel may have a second width. The first width may be smaller than the second width. A first conductor in the first channel may have a first conductor width. A second conductor in the second channel may have a second conductor width. The first conductor width may be substantially equivalent to the second conductor width. A spacer dielectric may be introduced on a side of the second channel.

In an embodiment, this disclosure relates to a method of manufacture of a semiconductor device. The method may include multiple-patterning the semiconductor device. The method may include establishing a signal conductor layer including a first channel defined by a first mask and a second channel defined by a second mask. The first channel may have a first width and the second channel may have a second width. The first width may be smaller than the second width. The method may include introducing a spacer dielectric on a side of the second channel. The method may include introducing a first conductor in the first channel having a first conductor width. The method may include introducing a second conductor in the second channel having a second conductor width. The first conductor width may be substantially equivalent to the second conductor width.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a cross-sectional view of a semiconductor device according to an embodiment;

FIG. **2** is a flow chart showing an operation to manufacture a semiconductor device according to an embodiment;

FIG. **3** is a flow chart showing an operation to manufacture a semiconductor device according to an embodiment;

FIG. **4**A is a flow chart showing an operation to manufacture a semiconductor device according to an embodiment;

FIG. **4**B illustrates applying a photoresist material according to an embodiment;

FIG. **4**C illustrates applying a mask and exposing photoresist material according to an embodiment;

FIG. **4**D illustrates developing exposed photoresist material according to an embodiment;

FIG. **4**E illustrates etching a channel according to an embodiment;

FIG. **4**F illustrates removing photoresist material according to an embodiment;

FIG. **4**G illustrates applying a photoresist material according to an embodiment.

FIG. **4**H illustrates applying a mask and exposing photoresist material according to an embodiment;

FIG. **4**I illustrates developing exposed photoresist material according to an embodiment;

FIG. **4**J illustrates etching a channel according to an embodiment;

FIG. **4**K illustrates removing photoresist material according to an embodiment;

FIG. **4**L illustrates determining widths, calculating differences, and depositing a dielectric material according to an embodiment;

FIG. **4**M illustrates an applying of a photoresist material according to an embodiment;

FIG. **4**N illustrates an exposing of the photoresist material and the dielectric material according to an embodiment;

FIG. **4**O illustrates a wet etch of the exposed dielectric material according to an embodiment;

FIG. **4**P illustrates a removal of the photoresist material according to an embodiment;

FIG. **4**Q illustrates an anisotropic etch of dielectric material according to an embodiment;

FIG. **4**R illustrates a conductor filling the trenches according to an embodiment;

FIG. **5**A is a flow chart showing an operation to manufacture a semiconductor device according to an embodiment;

FIG. **5**B illustrates determining widths, calculating differences, and depositing a dielectric material according to an embodiment;

FIG. **5**C illustrates an exposing of the photoresist material according to an embodiment;

FIG. **5**D illustrates a developing and a hardening of undeveloped photoresist material resulting in a hardened photoresist material according to an embodiment;

FIG. **5**E illustrates a depositing of a dielectric material according to an embodiment;

FIG. **5**F illustrates anisotropically etching dielectric material according to an embodiment;

FIG. 5G illustrates a removal of the hardened photoresist material which may be completed via plasma ashing according to an embodiment; and

FIG. 5H illustrates a conductor filling the trenches according to an embodiment.

DETAILED DESCRIPTION

A wiring track on a given plane of a semiconductor device may be designed to lithography and dielectric breakdown specifications. As conductor line width and pitch geometries decrease, the use of double-patterning on a particular level may increase in order to achieve the required conductor dimensions while still using existing state of the art lithographic exposure equipment. A benefit of double-patterning includes the ability to form tight conductor pitches; however, double-patterning may introduce other variables related to timing and noise into the semiconductor process. Double-patterns alter relationships between adjacent wires in both width and spacing. Adjacent wire channels may be defined in separate lithography steps. Distinctions between adjacent wires may arise due to lithographic exposure variations and registration or placement errors of one exposure relative to another. Aspects of the disclosure may limit the implications of such distinctions. Aspects of the disclosure may reduce lateral capacitance and signal coupling on a wiring track adapted to carry a signal.

Single level patterning enables straightforward characterization of parameters with signal delay implications such as wire width, height, and spacing variations. A product of a resistance value (R) of a wire and a capacitance value (C) of the wire forms an RC time constant for the wire (note this is an approximation since the R and the C are distributed along the wire length). Historically, a decrease in wire width or thickness brings about a resistance increase and a corresponding capacitance decrease. The C decrease approximately offsets the R increase in the RC time constant. Such capacitance decrease occurs in part due to a reduction in lateral capacitance because the space between wires increases as wire width decreases. Similarly, an increase in wire width or thickness brings about a resistance decrease approximately offset in the RC time constant by a corresponding capacitance increase. Such a capacitance increase occurs in part due to a rise in lateral capacitance because the space between wires decreases as wire width increases. Thus, in conventional, single-patterned wires the RC time constant remains within appropriate limits of tolerance.

Double-patterning may have different technical characteristics such as lateral capacitance relative to single level patterning. In double-patterning, the width of adjacent wires is rather independent, i.e., track poorly. Wire widths may not track well between adjacent wires created using separate exposures. Relatively narrow wires may be next to or between relatively wide wires. Double-patterning creates varying lateral capacitance between adjacent wires effectively separate from wire resistance variations. The resistance value (R) and the capacitance value (C) may fail to counterbalance each other across process variations. For example, a highly resistive wire may have high R and high C. Thus, the RC time constant between adjacent wires may vary significantly. Wires of one pattern of a double-pattern may carry a signal faster than wires of the other pattern. This may cause signals to reach their respective destinations at different times. Early analysis of a particular 14-15 nm technology indicates a potential doubling of worst case lateral capacitance between adjacent wires, doubling of coupled noise, and increased total wire C by as much as 50%. Such variations may require a solution to mitigate these effects. Adapting the wiring tracks to carry wires of substantially equivalent widths may achieve desirable results related to signal timing.

Aspects of the disclosure may include a signal conductor layer. The signal conductor layer may be a metal layer. The signal conductor layer may include channels which may be established. The channels may be trenches or troughs and may be defined by masks. The masks may be photomasks. The channels may include a first channel and a second channel. The first channel may have a first width. The second channel may have a second width. The first channel may be a result of a first channel pattern. The second channel may be a result of a second channel pattern.

In embodiments, a channel may include a dielectric material which may be introduced. The dielectric material of the channel may be a spacer. Where the dielectric material is not part of one of the channels, the channel may include a conductor which may be introduced. Aspects may include a first conductor in the first channel having a first conductor width. Aspects may include a second conductor in the second channel having a second conductor width. In embodiments, the first conductor width may be substantially equivalent to the second conductor width.

FIG. **1** illustrates a cross-sectional view of a semiconductor device according to an embodiment. The semiconductor device may be double-patterned. The semiconductor device may include a signal conductor layer **100**. The signal conductor layer may be a metal layer. The signal conductor layer may include a dielectric material. The signal conductor layer may include an oxide. Particular dielectric materials such as silicon dioxide may be used, though others are considered.

The signal conductor layer **100** may include a channel. A channel may be a trench. The channel may be adapted to hold a wiring track or wire which may be adapted to carry a signal or deliver power. In particular, the signal conductor layer **100** may include a first channel **110**. The first channel **110** may be a trench. The first channel **110** may be defined by a first mask. The first channel **110** may be a result of a first channel pattern. The first channel **110** may have a height **131** and a width **132**. The first channel **110** may include a conductor **101**A. The conductor **101**A may have a height **131** and a width **132**.

Also, the signal conductor layer **100** may include a second channel **120**. The second channel **120** may be a trench. The second channel **120** may be defined by a second mask. The second channel **120** may be a result of a second channel pattern. The second channel **120** may have the height **131** and a width **133**. The second channel **120** may include a conductor **101**B. The conductor **101**B may have the height **131** and the width **132**. The width **132** of the conductor **101**A of the first channel **110** may be substantially equivalent to the width **132** of the conductor **101**B of the second channel **120**. A substantially equivalent width may be a measurement of a first width within ten percent of a measurement of a second width. In embodiments, as depicted, the width may be the same. The two conductors, **101**A and **101**B, may be separately made to have the substantially equivalent width. The two conductors, **101**A and **101**B, may be designed to have the same width. Process tracking from a mask and an exposure may cause the two conductors, **101**A and **101**B, to be set to have different widths. In embodiments, aspects described may reduce lateral capacitance. In embodiments, aspects described may reduce signal coupling. In embodiments, aspects described may assist with signal timing.

In embodiments, a wider channel such as the second channel **120** in FIG. **1** may include a spacer dielectric **121**. Presence of the spacer dielectric **121** may reduce lateral capacitance, reduce signal coupling, or assist with signal timing.

The spacer dielectric **121** may be located on at least one vertical side of the second channel **120**. The spacer dielectric **121** may have a permittivity. The permittivity may be a relative permittivity and may be denoted as $\in_r(\omega)$ (sometimes κ or K) and may be defined as

$$\varepsilon_r(\omega) = \frac{\varepsilon(\omega)}{\varepsilon_0},$$

where $\in(\omega)$ is a complex frequency-dependent absolute permittivity of the material, and $\in_0$ is a vacuum permittivity. The permittivity of the spacer dielectric **121** may be less than the permittivity of silicon dioxide which may be 3.9. In embodiments, the spacer dielectric **121** may have a permittivity of 2.3 or a similar permittivity of less than 3.0.

In embodiments, the spacer dielectric has a total width substantially equivalent to a difference of the width **133** of the second channel **120** and the width **132** of the first channel **110**. The total width may be a sum of all widths of the spacer dielectric in a channel such as the second channel **120**. Capacitive coupling may be influenced by altering a size, such as a width, of the spacer dielectric **121**. In embodiments, the spacer dielectric **121** may be as thick as required to make up the capacitive difference between conductors in the channels. In embodiments, the permittivity of the spacer dielectric **121** may correlate with widths involved. In embodiments, the permittivity of the spacer dielectric **121** may be close to that of the signal conductor layer **100**. As such, in embodiments, conductor widths and therefore resistance may be substantially equivalent between the channels. In embodiments, the spacer dielectric **121** may not be an equivalent dielectric material to that of the signal conductor layer **100**. Other possibilities regarding the spacer dielectric **121** are considered, including using flourine-doped silicon dioxide, using carbon-doped silicon dioxide, placing the spacer dielectric **121** on a bottom surface of the channel, or varying the widths involved.

FIG. **2** is a flow chart showing an operation **200** to manufacture a semiconductor device according to an embodiment. At block **210**, operation **200** may include establishing a signal conductor layer having a first channel defined by a first mask and a second channel defined by a second mask. The first channel may have a first width and the second channel may have a second width. The first width may be smaller than the second width. At block **220**, operation **200** may include introducing a spacer dielectric on a side of the second channel. At block **230**, operation **200** may include introducing a first conductor in the first channel having a first conductor width. At block **240**, operation **200** may include introducing a second conductor in the second channel having a second conductor width. The first conductor width may be substantially equivalent to the second conductor width. A substantially equivalent width may be a measurement of a first width within ten percent of a measurement of a second width.

In embodiments, aspects described may reduce lateral capacitance. In embodiments, aspects described may reduce signal coupling. In embodiments, aspects described may assist with signal timing. In addition to the described, other embodiments having fewer steps, more steps, or different steps are contemplated. Also, some embodiments may perform some or all of the steps in FIG. **2** in a different order.

FIG. **3** is a flow chart showing an operation **300** to manufacture a semiconductor device according to an embodiment. At block **310**, operation **300** may include establishing a signal conductor layer. The signal conductor layer established at block **310** may be multiple-patterned. For example, the signal conductor layer established at block **310** may be double-patterned. At block **320**, operation **300** may include determining widths of channels. Determining widths may include determining a first width of the first channel and determining a second width of the second channel. Calculating a difference in the first width and the second width may also be included at block **320**.

At block **330**, operation **300** may include introducing a dielectric material. At block **340**, operation **300** may include introducing a photoresist material. At block **350**, operation **300** may include exposing at least a portion of at least one of the dielectric material and the photoresist material. In embodiments, the exposing may include not underexposing. In embodiments, the exposing may include overexposing where overexposing may include dimensions exposed, time, focus, etc. At block **360**, operation **300** may include removing a portion of the dielectric material. Presence of the dielectric material remaining may reduce lateral capacitance, reduce signal coupling, or assist with signal timing. Capacitive coupling may be influenced by altering a size, such as a width, of the dielectric material remaining. At block **370**, operation **300** may include removing the photoresist material. At block **380**, operation **300** may include introducing a conductive material. In embodiments, a first conductive material width associated with the first trench may be substantially equivalent to a second conductive material width associated with the second trench. Operation **400** of FIG. **4**A and operation **500** FIG. **5**A may describe operation **300** with further details. In addition to the described, other embodiments having fewer steps, more steps, or different steps are contemplated. Also, some embodiments may perform some or all of the steps in FIG. **3** in a different order.

FIG. **4**A is a flow chart showing an operation **400** to manufacture a semiconductor device according to an embodiment. At block **401**, operation **400** may include establishing (e.g., defining and etching) a signal conductor layer. The signal conductor layer established at block **401** may be multiple-patterned. For example, the signal conductor layer established at block **401** may be double-patterned. See FIGS. **4**B-**4**K. At block **402**, operation **400** may include determining widths of channels. Determining widths may include determining a first width of the first channel and determining a second width of the second channel. Calculating a difference in the first width and the second width may also be included at block **402**. At block **403**, operation **400** may include introducing (e.g., blanket depositing) a dielectric material. See FIG. **4**L.

At block **404**, operation **400** may include introducing (e.g., applying) a photoresist material. See FIG. **4**M. At block **405**, operation **400** may include exposing the photoresist material and the dielectric material of trenches that may not contain a spacer by applying a mask. In embodiments, the exposing may include not underexposing. In embodiments, the exposing may include overexposing where overexposing may include dimensions exposed, time, focus, etc. See FIG. **4**N. At block **406**, operation **400** may include removing (e.g., wet etching) exposed dielectric material (e.g., trenches that may not contain a spacer). See FIG. **4**O. At block **407**, operation **400** may include removing the photoresist material. See FIG. **4**P. At block **408**, operation **400** may include removing (e.g., anisotropic etching) dielectric material not existing as a spacer dielectric. See FIG. **4**Q. At block **409**, operation **400** may include introducing (e.g., filling trenches with, polishing) a conductive material. See FIG. **4**R. In addition to the described, other embodiments having fewer steps, more steps, or different steps are contemplated. Also, some embodiments may perform some or all of the steps in FIG. **4**A in a different order.

FIGS. **4**B-**4**R each illustrate a cross-sectional view of a semiconductor device according to an embodiment. FIGS. **4**B-**4**R each illustrate a "before and after" view of operation **400** at each block of FIG. **4**A according to an embodiment. Generally, FIGS. **4**B-**4**K illustrate a defining and an etching of the first channel **110** and the second channel **120** in the signal conductor layer **100** which is double-patterned according to an embodiment. The first channel **110** and the second channel **120** may each have the height **131**. The first channel **110** may have the width **132**. The second channel **120** may have the width **133**.

FIG. **4**B illustrates applying a photoresist material **410** according to an embodiment. FIG. **4**C illustrates applying a first mask **491** to begin defining a first channel with exposed photoresist material **411** according to an embodiment. FIG. **4**D illustrates developing the exposed photoresist material **411** according to an embodiment. The width **132** may not be to the exact dimensions of the first mask **491** due to variation in exposure time, focus, etc. FIG. **4**E illustrates etching the first channel **110** of the width **132** and a depth or height **131** according to an embodiment. FIG. **4**F illustrates removing the photoresist material **410** according to an embodiment.

FIG. **4**G illustrates applying a photoresist material **415** according to an embodiment. FIG. **4**H illustrates applying a second mask **492** to begin defining a second channel with exposed photoresist material **416** according to an embodiment. FIG. **4**I illustrates developing the exposed photoresist material **416** according to an embodiment. In embodiments, the width **133** may not be to the exact dimensions of the second mask **492** due to variation in exposure time, focus, etc. In embodiments where the dimensions of the first mask **491** and the second mask **492** are equivalent, the widths **132** and **133** may not be equivalent. FIG. **4**J illustrates etching the second channel **120** of the width **133** and a depth or height **131** according to an embodiment. FIG. **4**K illustrates removing the photoresist material **415** according to an embodiment. FIGS. **4**B-**4**K may be generally considered an example double-patterning operation, other multiple-patterning operations are considered.

FIG. **4**L illustrates determining a first width of the first channel and determining a second width of the second channel. A difference in channel widths may be calculated. FIG. **4**L further illustrates depositing a dielectric material **420** to the semiconductor device according to an embodiment. In embodiments, the dielectric material **420** may not be an equivalent dielectric material to that of the signal conductor layer **100**. The dielectric material deposited may be of a thickness substantially equivalent to half the difference. FIG. **4**M illustrates an applying of a photoresist material **430** to the semiconductor device according to an embodiment. FIG. **4**N illustrates an exposing of the photoresist material **430** and the dielectric material **420** of the first channel **110** which is a trench that may not contain a spacer. In embodiments, the exposing may include not underexposing. In embodiments, the exposing may include overexposing where overexposing may include dimensions exposed, time, focus, etc. The first mask **491** may be applied during a photolithographic process. After the photolithographic process, exposed photoresist material **431** and exposed dielectric material **421** may remain.

FIG. **4**O illustrates a wet etch of the exposed dielectric material **421**. The exposed photoresist material **431** may also be removed. FIG. **4**P illustrates a removal of the photoresist material **430**. FIG. **4**Q illustrates an anisotropic etch of the dielectric material **420** except for that which may exist as the spacer dielectric **121** on a side of a trench. The width **132** may be a horizontal width in the trench between the spacer dielectric **121** on the sides of the trench in an embodiment. FIG. **4**R illustrates a conductor **101** (i.e., **101**A in the first channel **110**, **101**B in the second channel **120**) filling the trenches. The conductor **101** may extend the height **131**. The conductor **101** may extend the width **132**. The finished product may be the same as FIG. **1**.

FIG. **5**A is a flow chart showing an operation **500** to manufacture a semiconductor device according to an embodiment. At block **501**, operation **500** may include establishing (e.g., defining and etching) a signal conductor layer. The signal conductor layer established at block **501** may be multiple-patterned. For example, the signal conductor layer established at block **501** may be double-patterned. Block **501** of operation **500** may be similar to or the same as block **401** of operation **400**. See FIGS. **4**B-**4**K. At block **502**, operation **500** may include determining widths of channels. Determining widths may include determining a first width of the first channel and determining a second width of the second channel. Calculating a difference in the first width and the second width may also be included at block **502**. At block **503**, operation **500** may include introducing (e.g., applying) a photoresist material. See FIG. **5**B.

At block **504**, operation **500** may include exposing the photoresist material of trenches that may not contain a spacer by applying a mask. In embodiments, the exposing may include not underexposing. In embodiments, the exposing may include overexposing where overexposing may include dimensions exposed, time, focus, etc. See FIG. **5**C. At block **505**, operation **500** may include developing and may include hardening undeveloped photoresist material. Hardening undeveloped photoresist material may improve adhesion of the photoresist material to the signal conductor layer. See FIG. **5**D. At block **506**, operation **500** may include introducing (e.g., blanket depositing) a dielectric material. See FIG. **5**E. At block **507**, operation **500** may include removing (e.g., anisotropically etching) dielectric material. See FIG. **5**F. At block **508**, operation **500** may include removing (e.g., plasma ashing) the photoresist material. See FIG. **5**G. At block **509**, operation **500** may include introducing (e.g., filling trenches with, polishing) a conductive material. See FIG. **5**H. In addition to the described, other embodiments having fewer steps, more steps, or different steps are contemplated. Also, some embodiments may perform some or all of the steps in FIG. **5**A in a different order.

FIGS. **5**B-**5**H each illustrate a cross-sectional view of a semiconductor device according to an embodiment. FIGS. **5**B-**5**H each illustrate a "before and after" view of operation **500** at each block of FIG. **5**A according to an embodiment. Before illustration FIG. **5**B, a double-patterned signal conductor layer may be established. FIGS. **4**B-**4**K illustrate a defining and an etching of the first channel **110** and the second channel **120** in the signal conductor layer **100** which is double-patterned according to an embodiment. The first channel **110** and the second channel **120** may each have the height **131**. The first channel **110** may have the width **132**. The second channel **120** may have the width **133**. Operations as depicted in FIG. **5**B may commence thereafter.

FIG. **5**B illustrates determining a first width of the first channel and determining a second width of the second channel. A difference in channel widths may be calculated. FIG. **5**B further illustrates an applying of a photoresist material **520** to the semiconductor device according to an embodiment. FIG. **5**C illustrates an exposing of the photoresist material **520** of the second channel **120** which is a trench that may contain a spacer. The second mask **492** may be applied during a photolithographic process. After the photolithographic process, exposed photoresist material **542** may remain. FIG. **5**D illustrates a developing and a hardening of undeveloped photoresist material resulting in a hardened photoresist material **550**. Hardening undeveloped photoresist material may improve adhesion of the photoresist material to the signal conductor layer.

FIG. **5**E illustrates a depositing of a dielectric material **560** to the semiconductor device according to an embodiment. The dielectric material deposited may be of a thickness substantially equivalent to half the difference calculated as shown in FIG. **5**B. FIG. **5**F illustrates anisotropically etching the dielectric material **560** except for that which may exist as the spacer dielectric **121** on a side of a trench and unsupported dielectric material **570**. The width **132** may be a horizontal width in the trench between the spacer dielectric **121** on the sides of the trench in an embodiment. FIG. **5**G illustrates a removal of the hardened photoresist material **550** which may be completed via plasma ashing. The unsupported dielectric material **570** may also disappear which may be as a result of the plasma ashing. FIG. **5**H illustrates a conductor **101** (i.e., **101**A in the first channel **110**, **101**B in the second channel **120**) filling the trenches. The conductor **101** may extend the height **131**. The conductor **101** may extend the width **132**. The finished product may be the same as FIG. **1**.

In the foregoing, reference is made to various embodiments. It should be understood, however, that this disclosure is not limited to the specifically described embodiments. Instead, any combination of the described features and elements, whether related to different embodiments or not, is contemplated to implement and practice this disclosure. Many modifications and variations may be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. Furthermore, although embodiments of this disclosure may achieve advantages over other possible solutions or over the prior art, whether or not a particular advantage is achieved by a given embodiment is not limiting of this disclosure. Thus, the described aspects, features, embodiments, and advantages are merely illustrative and are not considered elements or limitations of the appended claims except where explicitly recited in a claim(s).

What is claimed is:

1. A method of manufacturing a semiconductor device, comprising:

establishing a signal conductor layer formed of an insulator, the signal conductor layer having adjacent channels for wiring tracks, the adjacent channels including:

a first channel defined by a first mask having a design width and a second channel defined by a second mask having the design width, the first channel processed having a first width and the second channel processed having a second width, the first width smaller than the second width, a difference between the first width and the second width caused by tracking;

introducing a spacer dielectric on a side of the second channel, the spacer dielectric touching the insulator and bordered on at least two edges by the insulator;

introducing a first conductor in the first channel having a first conductor width, the first conductor touching the insulator and bordered on at least three edges by the insulator; and

introducing a second conductor in the second channel having a second conductor width, the second conductor touching the insulator and touching the spacer dielectric, the second conductor bordered on at least one edge by the insulator, the first conductor width substantially equivalent to the second conductor width.

2. The method of claim **1**, wherein the side is a vertical side.

3. The method of claim **2**, wherein the spacer dielectric has a permittivity less than 3.0.

4. The method of claim **2**, wherein the spacer dielectric has a total width substantially equivalent to the difference between the second width and the first width.

5. A method of manufacturing a semiconductor device, comprising:

establishing a signal conductor layer formed of an insulator, the signal conductor layer having adjacent trenches for wiring tracks, the adjacent trenches including:

defining a first portion of the signal conductor layer with a first mask and defining a second portion of the signal conductor layer with a second mask the first mask having a first pattern, including a design width, for a first trench and the second mask having a second pattern, including the design width, for a second trench, the first trench processed having a first trench width and the second trench processed having a second trench width, the first trench width smaller than the second trench width, a difference between the first trench width and the second trench width caused by tracking;

introducing a spacer dielectric material to the second trench, the first trench not including the spacer dielectric material;

introducing a photoresist material to at least one of the signal conductor layer and the spacer dielectric material;

exposing at least a portion of at least one of the spacer dielectric material and the photoresist material;

removing a first portion of the spacer dielectric material and retaining a second portion of the spacer dielectric material, the second portion of the spacer dielectric material having a thickness substantially equivalent to half the difference of the first trench width and the second trench width;

removing the photoresist material; and

introducing a conductive material to the signal conductor layer wherein a first conductive material width associated with the first trench is substantially equivalent to a second conductive material width associated with the second trench, the first conductive material bordered on at least three edges by the insulator.

6. The method of claim **5**, wherein introducing the spacer dielectric material includes blanket depositing the spacer dielectric material.

7. The method of claim **5**, wherein removing the first portion of the spacer dielectric material includes wet etching the portion of the spacer dielectric material exposed.

8. The method of claim **5**, wherein removing the first portion of the spacer dielectric material and retaining the second portion of the spacer dielectric material includes anisotropically etching the spacer dielectric material except for that which exists as a spacer on a side of the second trench.

9. The method of claim **5**, wherein removing the photoresist material includes plasma ashing the photoresist material.

10. The method of claim **5**, wherein exposing at least the portion of the photoresist material includes at least one of developing the photoresist material and hardening undeveloped photoresist material.

11. The method of claim **5**, wherein exposing at least the portion of at least one of the spacer dielectric material and the photoresist material includes exposing at least a width of at least one of the first trench and the second trench.

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